ECE 457 - Multilayer Project

October 17, 2019
Lucas Nieuwenhout
1464836

Abstract

The objective of this lab is to learn about the methods and techniques used in the fabrication of micro-scale devices and use characterization equipment to test their functionality. This lab was completed using the resources of the NanoFAB at the University of Alberta and with help from the lab staff. The wafer fabricated has two aluminum conducting layers sputtered onto the wafer with a silicon nitride insulating layer in between. The alignment of the first aluminum layer and silicon nitride layer was ideal while the alignment of the second aluminum layer decreased the contact area of the via by 10%. The wafer contained many electrical devices including resistors, inductors, capacitors, via chains, Greek crosses and Kelvin crosses. These devices were characterized after the fabrication process was complete and it was found that the measured resistance was consistently higher than the theoretical values. I believe that the increased resistance can be attributed to a higher practical resistivity of aluminum. This is likely because the sputtered aluminum thin film in this lab is less dense than an ideal aluminum layer, creating more intrinsic resistance. The final widths of the devices were not able to be measured due to a technical error with the Zygo interferometer but it would likely be found that with an increase in device width or depth, there would be a corresponding decrease in resistance.

Introduction

Fabrication of micro- and nano-scale devices is an industry that is growing as the need for smaller, quicker, and more power efficient devices in the market and in research settings increases. The technologies and processes involved in micro fabrication allow for granular control of many important properties of the wafers that are produced. The goal of this lab is to learn the processes and techniques used in the micro fabrication of multilayer devices and how they impact the final device that is created. We also learned about the characterization techniques used to inspect the devices and verify their functionality. This lab was conducted using the resources and expertise of the University of Alberta NanoFAB and its staff.

The multilayer device that we created in this lab was designed to include a wide variety of structures focusing on integrated circuit components like resistors, inductors, capacitors and characterization structures like Kelvin and Greek crosses. many of these devices require multiple layers in order to function, so the wafer we created has a three layer structure, two aluminum layers to create the devices, insulated by an intermediate layer of silicon nitride. Aluminum was selected as our conductor layer because of it's good adhesion to oxide layers and low relative cost to other conductors while the silicon nitride was selected for it's high resistance to diffusion of water along with it's superior electrical characteristics.

The aluminum layers were applied using a Magnetron sputtering system and etched using a wet aluminum etchant technique. This was completed for the first and the third layers of the wafer. The middle silicon nitride layer was deposited using Plasma Enhanced Chemical Vapour Deposition(PEVCD) and etched using CH_4 in the Trion Reactive Ion Etcher(RIE). All three of these layers were patterned with a positive photoresist AZ 1512 and exposed using an ABM mask aligner before being developed with AZ 400K 1:4 developer. Deposition of thin films were completed by the NanoFAB lab staff independent of our lab sessions but the patterning and etching of the films were completed during our lab sessions.

The characterization of the wafers focused on the measuring of feature dimensions and electrical resistance of those features. The dimensional characterization of the features was conducted as the wafer was fabricated using the AlphaStep contact profilometer and Filmetrics optical profilometer to determine film thicknesses as well as using the Zygo optical profilometer after the wafer was completed. The passive electrical components on the wafer were measured using the Wentworth 4-point probing system to determine their resistances.

Experimental

The entirety of this lab was conducted within the University of Alberta NanoFAB located in the Electrical and Computer Engineering Research Facility. All equipment and materials used in this lab were provided by the NanoFAB and its staff. While a certain portion of the work was done by myself and my partner during the laboratory section, a large amount of work was done by the lab staff between sections to allow us to continue. The steps completed by the lab staff will be indicated and described in the experimental section as relevant. References will be made to Appendix D showing the cross-section of the wafer at that point in the lab with format “(L1,i)” representing step “i)" from “Lab 1”. Images of the alignment and etching can be seen in the Results section.

The manufacturing of the multilayer project begins with a silicon wafer. This silicon wafer is cut from a boule and cleaned using piranha solution, a 3:1 mixture of sulphuric acid and hydrogen peroxide. This process is completed in one of the compatible wet decks and eliminates any contaminates that may be deposited on the surface. A roughly 300nm layer of silicon dioxide is then formed on the surface of the wafer by thermal oxidation. The oxide is not deposited on the wafer but is formed out of the top layers of the wafer along with oxygen from the immediate atmosphere or from injected water.(L1, ii)

Aluminum is then sputtered onto the wafer using a Magnetron sputtering system to be used as the first conducting layer of the wafer design. The target of the system has to be burned in and the chamber must be brought down to approximately 10^{-6} to 10^{-3} Torr before the deposition can begin by pummelling the target with argon gas. This aluminum layer is designed to be roughly 100nm thick but was found to be 90nm thick on our wafer as measured by the AlphaStep contact profilometer after the wafer had been etched. The AlphaStep contact profilometer uses an extremely sensitive capacitive sensor attached to a stylus that measures the contours of the wafer. The prepping of the wafer and deposition of silicon oxide and aluminum up to this point was completed by the lab staff.(L1,iii)

To pattern the wafer, we pattern a temporary photoresist layer that will be completely removed after the aluminum layer is etched. A positive photoresist AZ 1512 as produced by MicroChemicals is used for the entirety of the lab and is developed by AZ400K 1:4 developer after exposure. The photoresist is applied and baked using the Cee 200CB Coat-Bake System. The wafer was placed onto the pedestal of the Cee 200CB and checked for centre before pouring 10-15ml of AZ 1512 photoresist on and beginning the spreading program. The spreading program consisted of spinning at 500rpm for 10s to spread the photoresist across the wafer and then 5000rpm for 40s to ensure an even coat across the wafer. After the wafer is spin-coated, it is baked at 100°C for 60s to remove any excess water from the photoresist, this hardens the photoresist and reduces the chance of the wafer sticking to the mask. The wafer is then left to rehydrate for 30-60s, reintroducing a small amount of water to the photoresist required for proper exposure.(L1,iv)[1]

The AZ 1512 photoresist is exposed and patterned using an ABM Contact Mask Aligner.(L1,v) This system allows you to align the wafers, and then expose them to UV light. Precise alignment is not

needed as this is the first patterned layer of the wafer but for subsequent layers the alignment performed with this machine is critical to functioning devices. The photoresist on the wafer is exposed to UV light(365nm and 405nm) with an intensity of 54.3mJ/cm^2 for 2.5s. This makes the photoresist more susceptible to the AZ 400K 1:4 developer used for development. The photoresist's sensitivity to UV light is the reason that the lithography section of the nanoFAB is lit using longer wavelength light than UV light.

The wafer is then developed in the AZ 400K 1:4 developer by submerging the wafer in a glass dish containing the developer, and agitating the solution to promote development and diffusion of reactants. The UV exposed photoresist will etch at a much faster rate than the other photoresist but it is important not to over or underdeveloped the pattern. The target for development is 40s but our wafer was developed for 42s before being removed from the dish to be rinsed thoroughly with water and dried with nitrogen.(L1,vi) The wafer was then inspected using the microscope to ensure that the photoresist was developed properly and the wafer was clean. Over or under development will be indicated by rounded corners on features: if convex corners are rounded then it is likely overdevelopment and if concave corners are rounded then it is likely underdeveloped but this depends on feature shape. If the wafer is overdeveloped then the entire photoresist application process must be repeated, but if the wafer is underdeveloped then it can just be redeveloped for a short period of time and re-examined. Our wafer was slightly underdeveloped but redeveloping it likely would have gone too far.(Figure 1)

With the pattern of the mask transferred to the photoresist, the pattern can now be etched into the aluminum layer beneath. The aluminum etchant used is a 16:1:1:1 mixture of phosphoric acid:nitric acid:acetic acid:water that will selectively etch the aluminum at a much higher rate than the photoresist. The aluminum etchant was put in a glass container in one of the compatible wet decks and the wafer was submerged and gently rocked for 4m18s until the desired pattern was visibly etched into the aluminum layer.(L1,vii) The wafer was then removed from the etchant, rinsed, and dried with water and nitrogen. To ensure that the aluminum was completely etched it was inspected with the microscope. The thickness of the aluminum and photoresist layers were measured using the AlphaStep contact profilometer and found to be 1.28µm. With the aluminum layer completely patterned, the remaining photoresist was cleaned off of the wafer by agitating it in an acetone bath for 60s, rinsing it with isopropyl alcohol(IPA) for 30s, cleaning it off with water and then drying with nitrogen.(L1,iix) The effectiveness of this cleaning was confirmed with the microscope.

The final step of the first lab section is to measure the final thickness of the patterned aluminum layer using the AlphaStep profilometer. The thickness of our bottom aluminum layer was measured to be 90nm.

To save time and to allow us to complete the more hands-on processes in the lab there is some initial prep work completed by the lab staff. The silicon nitride layer to be patterned in the second lab section is deposited onto the wafer using Plasma Enhanced Chemical Vapour Deposition(PECVD). This

process is implemented by flowing a source gas into the chamber containing the wafer and inducing a chemical reaction on the surface of the wafer using plasma. PECVD's advantage over standard CVD is the use of plasma to induce the reaction instead of heat, this reduces the temperature cycling stress put on the wafer. The silicon nitride layer is targeted to be 150nm and we measured it at a later point to be 156.61nm. In addition to the silicon nitride layer deposited, the lab staff also applied a monolayer of hexamethyldisilazane(HMDS). This is a hydrophobic layer applied using the YES HMDS Oven that significantly increases adhesion between the photoresist and non-metal films. The wafer was left to cool for 5 minutes and returned for our second lab section.(L2,iii)

The second lab section began with application of photoresist using the same process as for the aluminum layer.(L2,iv) The wafer was then secured to the ABM mask aligner as in the first lab and the second mask was affixed to the mask frame and secured with the mask vacuum. The substrate and mask were brought close to contact, levelled and gradually aligned using the alignment marks. Once alignment was achieved, the wafer was subjected to the same exposure treatment and developing process as the initial photoresist layer at 54.3mJ/cm^2 for 2.5s, and 43s respectively.(L2,vi) The wafer development was inspected and the thickness of the photoresist layer was measured using the AlphaStep to be 1.42µm.

The thickness of the silicon nitride layer was measured using the Filmetrics interferometer on a representative piece of silicon wafer that was deposited at the same time as our wafer.(L2,vii) This instrument uses the refractive and interference properties of light to determine the thickness of a thin film, determining the thickness of the film as a function of the wavelength of light and the angle of incidence. The thickness of the silicon nitride layer was found to be 156.61nm. Ideally this thickness would be used to determine the etching time, however an etching time of 140s was predetermined to ensure that all of the small features were etched correctly. The wafer was etched using CH_4 by a dry etch method in the Trion Reactive Ion Etcher(RIE). The wafer was placed onto the carbon chuck and the RIE was programmed to etch for 140s at an etch rate of approximately 267 nm/min. It should be noted that the etch rate is not actually 267 nm/min as the etch rate is not linear as it etches through the thin film.(L2,iix)

After the silicon nitride layer was etched, the photoresist was cleaned off of the wafer using the same process as in Lab 1.(L2,ix) We then measured the thickness of the silicon nitride using the AlphaStep profilometer. This gave a height of 216nm but we are not confident in this value as apparently the AlphaStep may be out of calibration and the Filmetrics value is more accurate.

Between the second and the third lab section the final aluminum thin film was applied to the wafer by the lab staff. This deposition uses the same process and parameters as the sputtering of the first aluminum layer.

The procedure of the third lab is very similar to the first lab, using all of the same processes in the same order. The AZ 1512 photoresist is applied using the Cee 200CB Coat-Bake system and patterned with the third layer mask using the ABM mask aligner as in the first lab. The photoresist layer was then developed for 44s, slightly longer than the target of 40s, however the wafer was not overdeveloped as

there wasn't full submersion for the first couple seconds of the development. The height of the photoresist layer was measured with the AlphaStep and found to be 1240nm.(L3,v)

The aluminum was etched using the same aluminum etchant as in the first lab. The duration of this etching process was significantly longer though at 7m28s as the same batch of etchant was used and the effectiveness of the solution had decreased. The wafer was rinsed with water and dried with nitrogen immediately after removal from the etchant.(L3,vi) The etched features were then inspected using the microscope and confirmed that there was no over or underdevelopment. As this is the final process, the photoresist layer was then removed with a longer 1m30s wash in acetone and 30s in IPA before rinsing with water and drying with nitrogen again.(L3,vii) The aluminum thickness was measured as 183.6nm using the AlphaStep profilometer.

The final lab section focused on characterization of the wafer and patterned features. We first used the Wentworth 4 point probing system to measure the resistances of the short 10µm resistor, long 10µm resistor, short via chain, long via chain, 10µm Greek cross and the 10µm Kelvin cross. This was done by supplying a voltage across two probes while reading the voltage across another set of probes, eliminating error introduced by probe resistance. The supply voltages and full data collected can be seen in Appendix A(Full Data). Finally, the features were then examined using the Zygo interferometer. This system uses the constructive and deconstructive interference of light to determine the profile of a surface and render a 3D model.

Results

The thickness of the applied thin film layer and photoresist were measured in each of the lab sections before and after etching. This allowed us to check the thickness of the photoresist to ensure that it will adequately protect the features that are not to be etched and that it has been developed in the areas to be etched.

The bottom aluminum layer photoresist was developed for 42s and measured to be 1205nm thick while the aluminum layer was etched for 4m18s and measured to be 90nm thick.(both measurements taken with AlphaStep) See Figure 1 and Figure 2 for the post develop and post etch images.

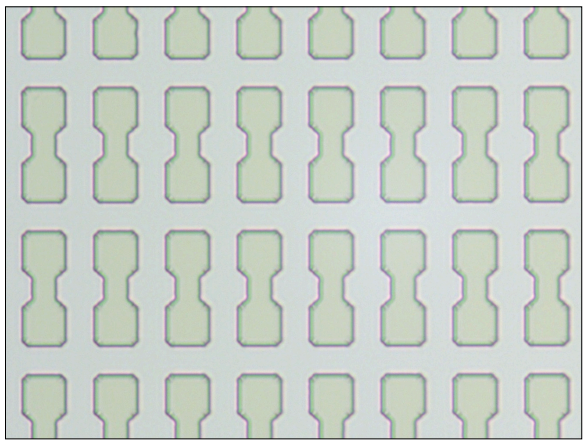


Figure 1: Lab 1 Post Develop Via Chain

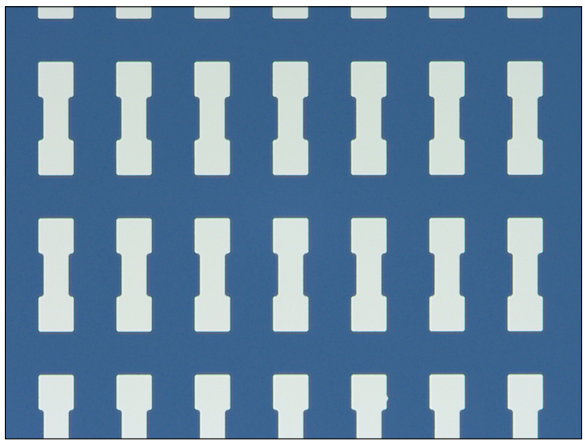


Figure 2: Lab 1 Post Etch Via Chain

The silicon nitride layer photoresist was developed for 43s and measured to be 1420nm thick(using AlphaStep) while the silicon nitride layer on a representative piece of wafer was measured to be 216nm(using Filmetrics). See Figure 3 and Figure 4 for the post develop and post etch images.

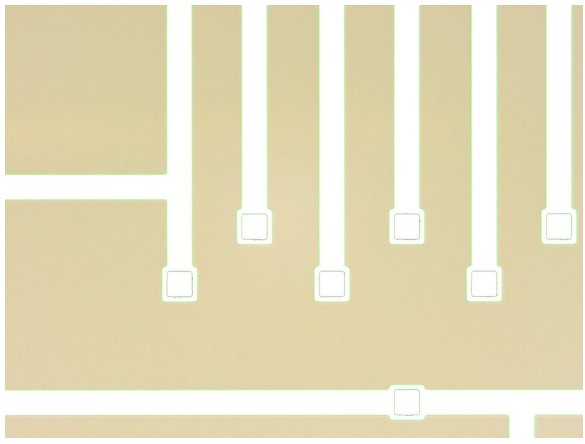


Figure 3: Lab 2 Post Develop Via

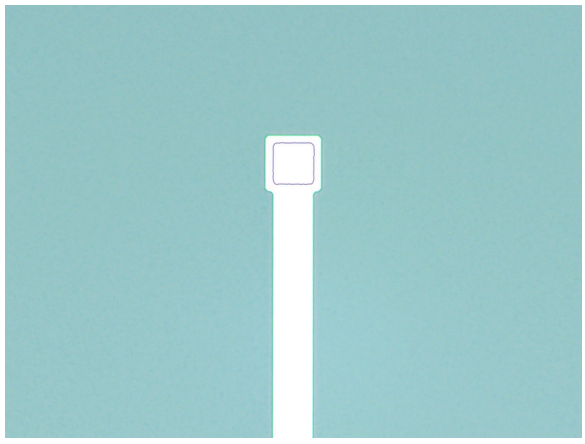


Figure 4: Lab 1 Post Etch Via

The top aluminum layer photoresist was developed for 44s and measured to be 1240nm thick while the aluminum layer was etched for 7m28s and measured to be 183nm thick.(both measurements taken with AlphaStep). See Figure 5 and Figure 6 for the post develop and post etch images.

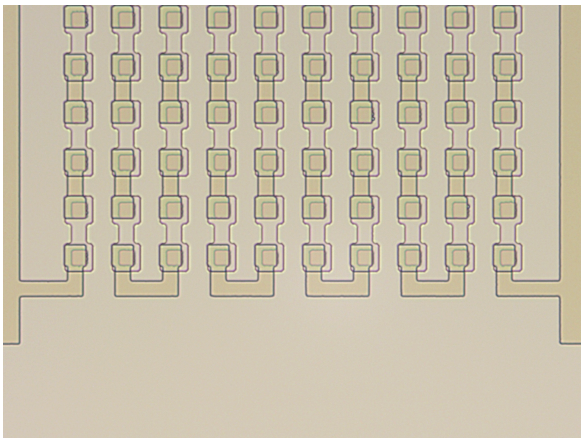


Figure 5: Lab 3 Post Develop Via Chain

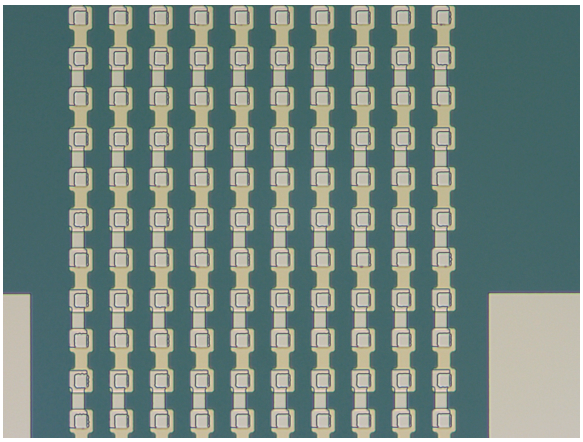


Figure 6: Lab 3 Post Etch Via Chain

The thin film layers were measured again using the Zygo interferometer in the final lab session. The measurements were made using the 3D model of the mask alignment marks as seen in Figure 7 and Figure 8 in Appendix B. The thicknesses of the layers as measured by the various profilometers can be seen in Table 1.

Profilometer:	AlphaStep			Filmetrics	Zygo
Measurand:	Photoresist Thickness [nm]	Photoresist and Thin Film Thickness [nm]	Thin Film Thickness [nm]	Thin Film Thickness [nm]	Thin Flim Thickness [nm]
Bottom Aluminum Film	1205	1280	90	-	469
Silicon Nitride Film	1420	-	216	156.61	200
Top Aluminum Film	1240	-	183	-	163

Table 1: Film Thicknesses as measured by AlphaStep, Filmetrics and Zygo profilometers

The short 10µm resistor and long 10µm resistor were measured using the Wentworth 4 point probe system at increments of 0.5V from 0V to 2.5V. The average resistance of the resistors can be calculated as the average of the individual resistances measured(Equation 1 and 3), or the slope of the trend line fit to the dataset(Equation 2 and 4). The full measurements are in Appendix A and the resulting charts can be seen as Figure 10 and Figure 11 in Appendix B. Error analysis can be found in Appendix E.

$$R_{Short,10\mu m,Average} = \frac{146.91\Omega + 146.90\Omega + 147.00\Omega + 147.05\Omega + 147.20\Omega}{5} = 147.01\Omega \quad (1)$$

$$R_{Short,10\mu m,Trendline} = \frac{1000}{6.7982\frac{mA}{V}} = 147.1\Omega \quad (2)$$

$$R_{Long,10\mu m,Average} = \frac{288.17\Omega + 288.72\Omega + 288.34\Omega + 288.67\Omega + 288.80\Omega}{5} = 288.54\Omega \quad (3)$$

$$R_{Long,10\mu m,Trendline} = \frac{1000}{3.4642\frac{mA}{V}} = 288.67\Omega \quad (4)$$

The long and short via chains were also measured with the Wentworth. The long via chain was found to be open circuit but the short via chain conducted properly. The total resistance of the via chain can be calculated using the same methods as the short resistor(Equation 5 and 6). Then the resistance of the short resistor must be subtracted from the total, and that number divided by the number of vias to determine the resistance of a single via. The measurements can be seen in Appendix A and the chart as Figure 12 in Appendix B.

$$R_{ShortViaChain,10\mu m,Average} = \frac{1848.15\Omega + 1880.38\Omega + 1891.14\Omega + 1877.36\Omega + 1878.79\Omega}{5} = 1875.16\Omega \quad (5)$$

$$R_{ShortViaChain,10\mu m,Trendline} = \frac{1000}{0.5319\frac{mA}{V}} = 1880.05\Omega \quad (6)$$

$$R_{Via,10\mu m,Average} = \frac{R_{ShortViaChain,10\mu m,Average} - R_{Short,10\mu m,Average}}{\#Vias} = \frac{1875.16\Omega - 147.01\Omega}{200} = 8.64\Omega \quad (7)$$

$$R_{Via,10\mu m,Trendline} = \frac{R_{ShortViaChain,10\mu m,Trendline} - R_{Short,10\mu m,Trendline}}{\#Vias} = \frac{1880.05\Omega - 147.10\Omega}{200} = 8.67\Omega \quad (8)$$

The 20µm Greek Cross and Kelvin Cross were measured using the Wentworth probing system to find the sheet and contact resistance respectively. Both of these features were successfully measured and the full data can be seen in Appendix A. The crosses can be rotated in increments of 90° and measured to determine the average resistance as in Equation 9, 10 and 11. The Greek Cross was measured in 4 orientations and the Kelvin Cross was measured in two orientations. The full data can be seen in Appendix A.

$$R_{SheetResistance,Greek} = \frac{0.706\Omega + 0.831\Omega + 0.702\Omega + 0.834\Omega}{4} = 0.768\Omega \quad (9)$$

$$R_{Via,20\mu m,Kelvin} = \frac{0.587\Omega + 0.586\Omega}{2} = 0.587\Omega \quad (10)$$

$$R_{Via,10\mu m,Kelvin} = \frac{R_{Via,20\mu m,Kelvin} * A_{20\mu m}}{A_{10\mu m}} = \frac{(0.587\Omega)(20\mu m)^2}{(10\mu m)^2} = 2.348\Omega \quad (11)$$

Discussion

The proper alignment of the thin film layers is essential to the operation and performance of the devices with exception of the first aluminum layer as there is no base pattern to align it with. The alignment of the silicon nitride layer is very important. This layer patterns the vias and insulation between the two aluminum layers. Our alignment of this layer worked very well as can be seen in Figure 3 and Figure 4. The pattern for the vias are completely centred on the contact pad of the aluminum. This ensures that there will be maximum surface contact between the first aluminum layer and the via. This also allows more leniency on alignment of the third layer, it is still critical that it is aligned well but a poor alignment of the third layer has less chance of complete device failure.

The alignment of the third layer was less accurate. I would estimate that the alignment is off 6 ± 1 µm in the x direction and 5 ± 1 µm in the y direction. This inaccuracy can be seen in Figure 5 and Figure 6 and in the final alignment marks of all three layers in Figure 9. There is an approximately 5µm margin of error in each direction for the alignment of the vias but as a result of the 6µm misalignment of the third layer the contact area of the via is reduced by 10%, leading to a higher resistance than designed. The likely reason for this misalignment is the slight shifting of the wafer during alignment between the application of the contact vacuum and release of the substrate vacuum. We aligned the wafer properly and checked the alignment after the vacuum was transferred but it was correctly judged to not be worth repeating the entire re-alignment, I believe that with a couple more attempts that we could have aligned it properly. If I were to design an alignment pattern I think I may add a sort of hatching pattern with known dimensions so that the misalignment could be quantified while aligning to see if it acceptable for the feature size of the wafer design.

During the characterization lab we tested the performance of the Short and Long 10µm resistors, Short and Long 10µm Via Chains, Small and Large 10µm Inductors, the 20µm Greek Cross and the 20µm Kelvin Cross. The data from this characterization is in Appendix A. All of these devices operated as expected with the exception of the Long 10µm Via Chain, which did not conduct at all. Further analysis of the results will be completed below, note that the trendline values, taken from Figures 10-12, will be used where possible to most accurately represent the data.

The Short 10µm Resistor was experimentally found to have a resistance of 147.1Ω(Equation 2), this is much higher than the theoretical resistance of 11.24Ω(Equation 13) when considering an aluminum thickness of 150nm as designed, or a resistance of 10.34Ω(Equation 12) when considering an aluminum thickness of 163nm as measured by the Zygo interferometer. There is a similar outcome with the Long 10µm resistor, the experimental resistance is 288.67Ω(Equation 4) while the 150nm thickness theoretical resistance is 22.45Ω(Equation 15) and the 163nm thickness theoretical resistance is 20.68Ω(Equation 15). This shows that the theoretical resistance of these resistors is consistently and significantly lower than the measured values in the lab. Since there are no vias or other features in this measuring setup, a 4 point probe is used, and there is no evidence of significant over-etching, it is most likely that the increased

resistance is caused by an increase to the actual resistivity of the aluminum. This may be caused by an inconsistent sputtering pattern or sputtering density. This is further supported by the correlation between the measured values of the Short and Long 10µm resistors. As the length of the resistor doubles, the resistance increases 196% from 147.1Ω to 288.67Ω. This suggests that this discrepancy between theoretical and measured values scales with resistor length and is not a fixed magnitude.

The 20µm Greek cross was also measured and resulted in a sheet resistance of 0.768Ω(Equation 9). This measured sheet resistance is much larger than the theoretical sheet resistance of 0.181Ω(Equation 21) when using 150nm thickness or 0.166Ω(Equation 20) when using 163nm thickness. The measured sheet resistance values do however correlate better with the measured resistances of the Short and Long 10µm resistors. When the Greek Cross measured sheet resistance is used to calculate the resistance of the Short and Long 10µm resistors as in Equation 14 and Equation 17 it is approximately ⅓ of the measured values of the resistors. This difference in resistance could be the result of determining the sheet resistance from a 20µm Greek cross and comparing it to 10µm resistors, even though sheet resistance should be independent of the Greek cross size it is possible that the error in this assumption was magnified by the length of the resistors.

Using the measurements from the 20µm Kelvin cross, it was calculated that the contact resistance of a 20µm via is 0.587Ω(Equation 10) while the contact resistance of a 10µm via is 2.348Ω(Equation 11). These resistances along with the sheet resistance measured in the Greek cross can be used to predict the resistances of the Short and Long Via Chains. This gives total via chain resistances of 517.37Ω(Equation 18) and 141.28Ω(Equation 19) for the Short and Long 10µm Via Chains respectively. This value is approximately 28% of 1880.05Ω, the measured resistance of the Short Via Chain. This is similar to the ⅓ discrepancy between the theoretical and measured values of the Short and Long 10µm resistors. This suggests that a majority of the increase in resistance of the via chains can also be attributed to a three times increase in the resistivity of the sputtered layer of aluminum relative to the ideal resistivity. The additional increase in resistance could be attributed to the poor alignment of the third layer, this would decrease the contact area by 10% as previously mentioned and increase the resistance.

Two of the inductors were also checked for functionality despite not having an LCR meter to measure their inductance. A voltage was applied across the small and the large spiral inductors and continuity was confirmed. The capacitors were not characterized as if functioning properly they would read open circuit but with further review it would have been beneficial to confirm this.

The overall yield of the wafer was very successful. We were able to test and measure all of the devices except for the long via chain. I believe that our alignment between the first and second layers was nearly flawless while our alignment between the second and third layers was slightly off and may have affected performance of the devices. I also believe that it is important that we properly developed the photoresist, if not, erring on the side of slightly over-developing as can be seen in Figures 1-6. This prevented any unwanted short circuits within or between devices. I do believe though that the photoresist

in the vias may have been slightly underdeveloped and this is causing a slightly smaller via contact area and increasing contact resistance. This could potentially be remedied by agitating the wafer more while developing it in the AZ 400K 1:4 developer to better pattern the small features. The main result of the measurement of the devices is that the measured resistance of the sputtered aluminum layer is much larger than the resistance of the same features using ideal aluminum. This may be improved by increasing the density of the sputtered aluminum films. As discussed in the lab, this could be done by heating the wafer to allow incident atoms to diffuse further after contact or by applying a bias to the wafer to attract some ions and cause re-sputtering. These techniques mostly improve the uniformity and smoothness of the sputtered film but will also increase the density.

The horizontal measurements taken with the Zygo interferometer give completely incorrect dimensions for the features on the wafer. The optical profilometer measured dimensions of features that are approximately ⅕ of the designed dimensions so all of the horizontal distances have been disregarded due to instrument error. The depth/thickness measurements made by the Zygo interferometer are in the last column of Table 1. These measurements seem to be more accurate than the horizontal distances but I suspect that they also have error contributed to them, specifically the thickness of the first layer. This is significantly higher than the AlphaStep measured thickness of 90nm.

Unfortunately without being able to measure the horizontal dimensions of the features on the wafer I cannot compare them to the theoretical values or justify the effect they may have had on the resistance or properties of the features. Generally for conductors, if the measured depth or width of the features is larger than the designed depth or width of the features, this will lead to a decrease in resistance due to the larger cross-section of the conductor or shorter path. The width and depth of an insulating layer has less of an effect on the resistance but increased via length or smaller via diameter could also increase resistance. The opposite is true for smaller conductor features, increasing the resistance compared to the designed values.

Capacitors will also be affected by the thickness and width difference between designed and measured. The capacitance relationship relies on the thickness of the film, the finger overlap and gap width as seen in Equation 22. A change in feature size due to over-etching would have little effect on the capacitance as the gap width and finger overlap would change proportionally, while an increase in film depth would increase capacitance. The inductance of the spiral inductors would not change drastically with an increase or decrease in feature size as the inductance relies on the number of spirals, radius of the spiral and the mean radius of the spiral(Equation 23), all of which would not change meaningfully with increases to conductor width or thickness.

$$C_{Single} = \frac{\epsilon t l}{g} \qquad (22)$$

$$L \approx \frac{45\mu_0 n^2 a^2}{22r - 14a} \qquad (23)$$

Conclusion

I believe that the goal of finding out more about the processes and techniques used in micro-fabrication was met by this lab. The multi-layer wafer was prepared, patterned, etched and finally characterized throughout the course of this lab using a wide variety of equipment and processes. The wafer had a high yield with only the Long Via Chain completely not functioning while the other components like the resistors, inductors, capacitors and crosses acted in a similar manner to the theory but with a higher than expected resistance in the aluminum conductor. This was likely caused by the imperfect density of the sputtered aluminum films along with some slightly misaligned layers. This could be improved by heating or applying a voltage potential to the wafer as it is being sputtered to increase the density and smoothness of the sputtered layers. The alignment likely didn't have as large of an effect on the increased resistance but could have made more of an impact if the thin films had been over-etched. Alignment is difficult to improve but allowing more time for more attempts at achieving the perfect alignment could increase the accuracy.

Bibliography

[1] MicroChemicals, Photoresist Rehydration. Accessed Oct. 12, 2019.[Online]. https://www.microchemicals.com/technical_information/photoresist_rehydration.pdf

[2] W..M Haynes, CRC Handbook of Chemistry and Physics. Boca Raton:CRC Press, 2009

Appendices

Appendix A - Full Measured Data

Short 10um Resistor				
Input Voltage [V]	Voltage Drop [V]	Current [A]	Current [mA]	Resistance [Ω]
0	0	0	0	N/A
0.5	0.476	0.00324	3.24	146.91
1	0.949	0.00646	6.46	146.90
1.5	1.423	0.00968	9.68	147.00
2	1.897	0.0129	12.9	147.05
2.5	2.364	0.01606	16.06	147.20
			Average of Resistance Points:	147.01Ω
			Trendline Resistance: (Figure 10)	147.10Ω

Table 2: Short 10µm Resistor Measurements

Long 10um Resistor				
Input Voltage [V]	Voltage Drop [V]	Current [A]	Current [mA]	Resistance [Ω]
0	0	0	0	N/A
0.5	0.487	0.00169	1.69	288.17
1	0.973	0.00337	3.37	288.72
1.5	1.459	0.00506	5.06	288.34
2	1.937	0.00671	6.71	288.67
2.5	2.423	0.00839	8.39	288.80
			Average of Resistance points:	288.54Ω
			Trendline Resistance: (Figure 11)	288.67Ω

Table 3: Long 10µm Resistor Measurements

Short Via Chain				
Input Voltage [V]	Voltage Drop [V]	Current [A]	Current [mA]	Chain Resistance [Ω]
0	0	0	0	N/A
0.5	0.499	0.00027	0.27	1848.15
1	0.9966	0.00053	0.53	1880.38
1.5	1.494	0.00079	0.79	1891.14
2	1.99	0.00106	1.06	1877.36
2.5	2.48	0.00132	1.32	1878.79
			Average of Resistance points:	1875.16
			Trendline Resistance: (Figure 12)	1880.05

Table 4: Short 10µm Via Chain Measurements

Greek Cross				
Orientation	Input Voltage [V]	Measured Voltage [V]	Current [A]	Sheet Resistance [Ω]
0°	1	0.0000055	0.0353	0.000706175
90°	1	0.0000055	0.03	0.000830933
180°	1	0.0000059	0.0381	0.000701862
270°	1	0.0000067	0.0364	0.000834253

Table 5: 20µm Greek Cross Measurements

Kelvin Cross					
Orientation	Input Voltage [V]	Measured Voltage [V]	Current [A]	Contact Resistance [Ω]	Specific Contact Resistivity[Ω/m]
0°	0.63	0.017714	0.03017	0.587139543	2.34856e-10
180°	0.63	0.0178	0.03035	0.586490939	2.34596e-10

Table 6: 20µm Kelvin Cross Measurements

Appendix B: Additional Figures

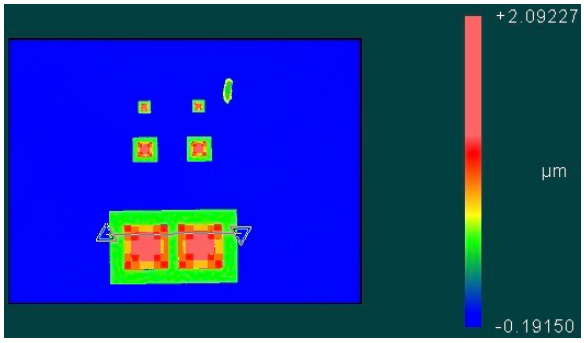


Figure 7: Alignment Mark Topography

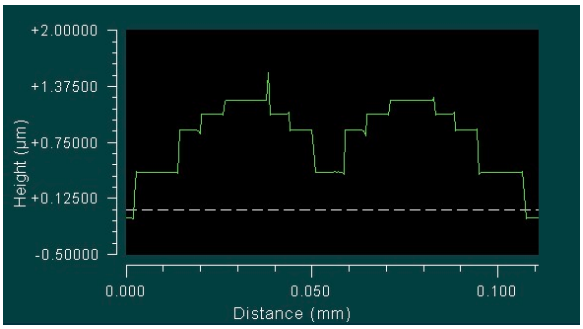


Figure 8: Alignment Mark Height

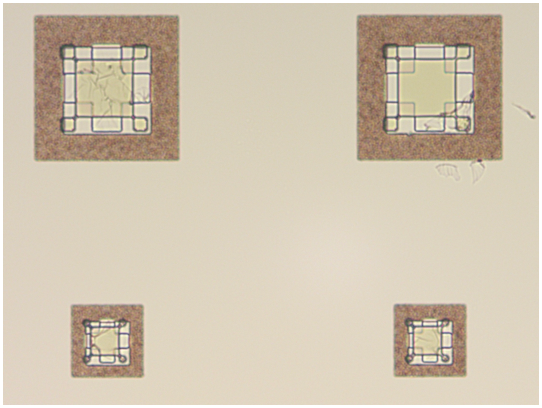


Figure 9: Alignment Marks Lab 3 Post Develop

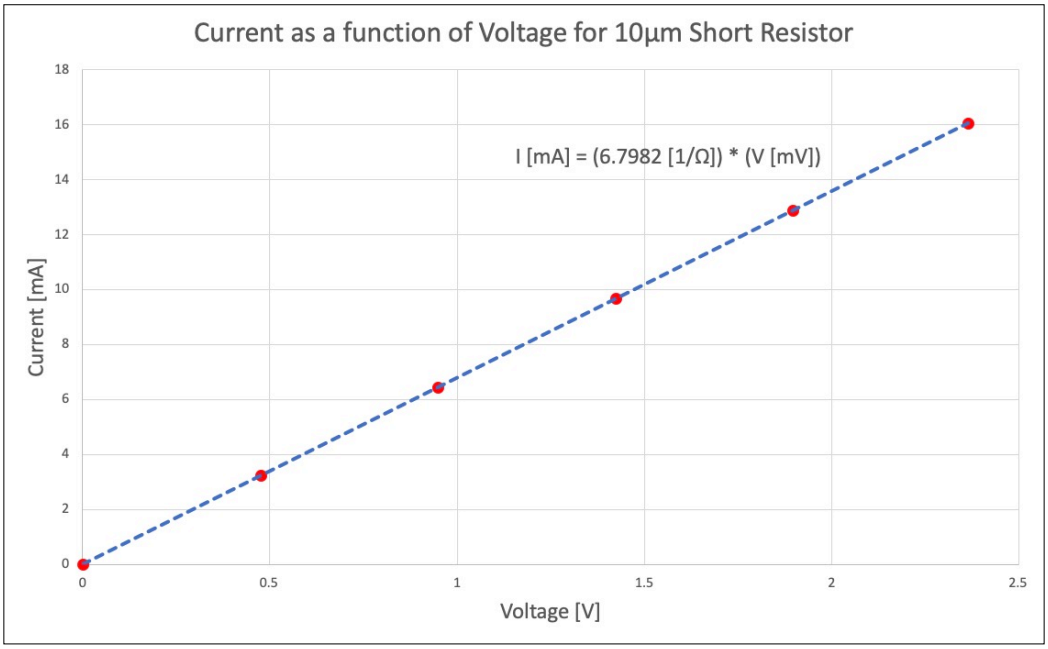


Figure 10: 4 point probe measurements of Short 10µm Resistor

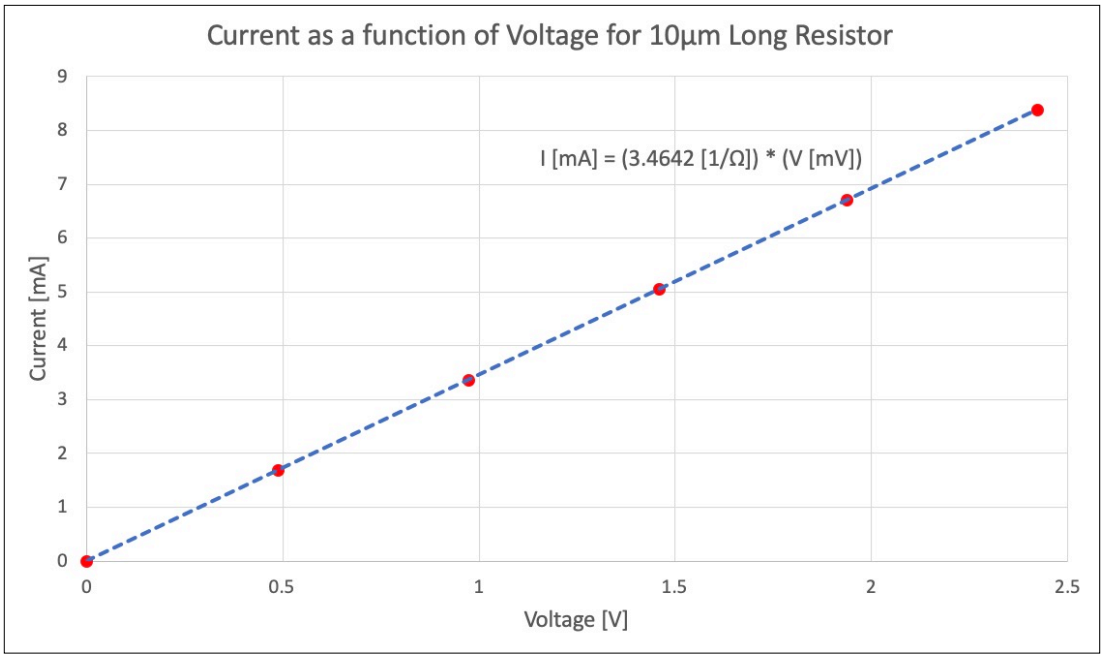


Figure 11: 4 point probe measurements of Long 10µm Resistor

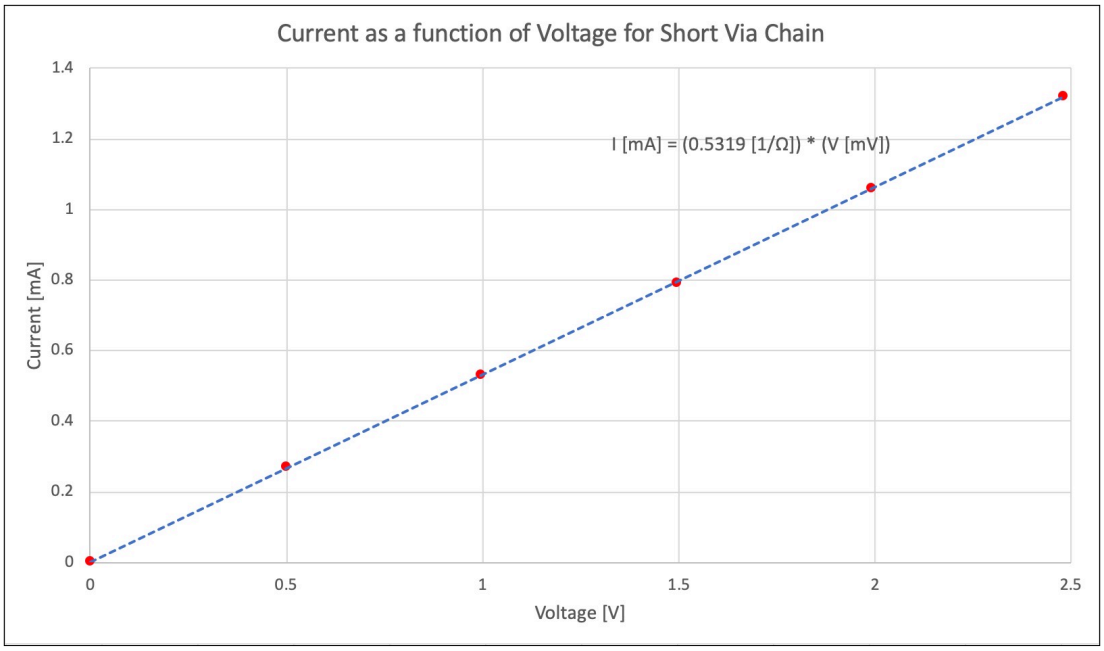


Figure 12: 4 point probe measurements of Short Via Chain

Appendix C: Additional Discussion Calculations

Short 10µm Resistor:

Resistance calculated using actual thin film thickness and theoretical resistivity[2]:

$$R_{Short,10\mu m,163nm,Theoretical} = \rho\frac{L}{Wt} = (2.71 * 10^{-8}\frac{\Omega}{m})\frac{622\mu m}{(10\mu m)(163nm)} = 10.34\Omega \qquad (12)$$

Resistance calculated using theoretical thin film thickness and resistivity[2]:

$$R_{Short,10\mu m,150nm,Theoretical} = \rho\frac{L}{Wt} = (2.71 * 10^{-8}\frac{\Omega}{m})\frac{622\mu m}{(10\mu m)(150nm)} = 11.24\Omega \qquad (13)$$

Resistance calculated using sheet resistance as measured in 20µm Greek Cross:

$$R_{Short,10\mu m,Sheet} = R_S\frac{L}{W} = (0.768\Omega)\frac{622\mu m}{10\mu m} = 47.77\Omega \qquad (14)$$

Long 10µm Resistor:

Resistance calculated using actual thin film thickness and theoretical resistivity[2]:

$$R_{Long,10\mu m,163nm,Theoretical} = \rho\frac{L}{Wt} = (2.71 * 10^{-8}\frac{\Omega}{m})\frac{1244\mu m}{(10\mu m)(163nm)} = 20.68\Omega \qquad (15)$$

Resistance calculated using theoretical thin film thickness and resistivity[2]:

$$R_{Short,10\mu m,150nm,Theoretical} = \rho\frac{L}{Wt} = (2.71 * 10^{-8}\frac{\Omega}{m})\frac{1244\mu m}{(10\mu m)(150nm)} = 22.48\Omega \qquad (16)$$

Resistance calculated using sheet resistance as measured in 20µm Greek Cross:

$$R_{Long,10\mu m,Sheet} = R_S\frac{L}{W} = (0.768\Omega)\frac{1244\mu m}{10\mu m} = 95.54\Omega \qquad (17)$$

Short 10µm Via Chain:

Resistance calculated using via and sheet resistance from Greek and Kelvin Crosses:

$$R_{ShortViaChain,10\mu m,Sheet} = R_S\frac{L}{W} + (\#Vias)R_{Via} = (0.768\Omega)\frac{622\mu m}{10\mu m} + (200)(2.348\Omega) = 517.37\Omega \qquad (18)$$

Long 10µm Via Chain:

Resistance calculated using via and sheet resistance from Greek and Kelvin Crosses:

$$R_{LongViaChain,10\mu m,Cross} = R_S\frac{L}{W} + (\#Vias)R_{Via} = (0.768\Omega)\frac{1244\mu m}{20\mu m} + (200)(0.587\Omega) = 141.28\Omega \qquad (19)$$

Greek Cross, 20µm:

Theoretical value of sheet resistance using actual film thickness[2]:

$$R_{Sheet,163nm,Theoretical} = \frac{\rho}{t} = \frac{2.71 * 10^{-8}\frac{\Omega}{m}}{163nm} = 0.166\Omega \qquad (20)$$

Theoretical value of sheet resistance using theoretical film thickness[2]:

$$R_{Sheet,150nm,Theoretical} = \frac{\rho}{t} = \frac{2.71 * 10^{-8}\frac{\Omega}{m}}{150nm} = 0.181\Omega \qquad (21)$$

Appendix D: Full Process Steps

Lab 1: Process Flow Cross-Section

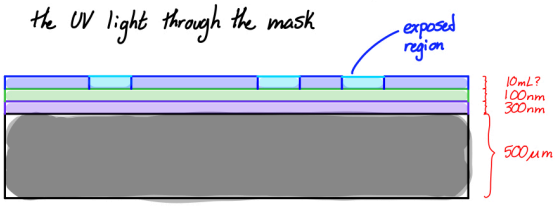
i) Just Substrate, cut from crystal, this is cleaned using a 3:1 mixture of H_2SO_4 and H_2O_2.

ii) Silicon Dioxide layer(approx 300nm) is grown using thermal oxidation

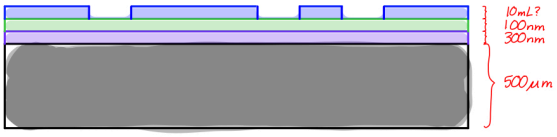
iii) Aluminum is deposited onto the wafer using a sputtering technique. (approx. 100nm)

iv) Photoresist layer is spin-coated onto the aluminum, This layer is sensitive to UV light. Approximately 10mL should be used.

v) A mask with the desired pattern is aligned with the wafer and the wafer is exposed to the UV light through the mask



vi) The wafer is then developed in a developing solution that dissolves the exposed photoresist. Ensure that the photoresist is properly developed.



vii) Etch the aluminum using the aluminum etchant for 4-8 minutes, visually inspecting for completion.

iix) Measure thickness using AlphaStep, wash off photoresist with acetone, then directly measure aluminum with AlphaStep

☆ Steps i) → iii) are completed upon arrival

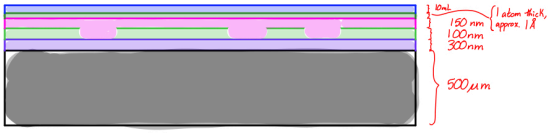
Lab 2: Process Flow Cross-Section

i) Start with aluminum patterned layer from the previous lab section.

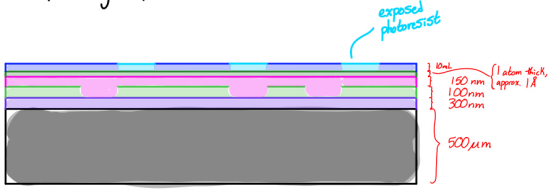
ii) PECVD Silicon Nitride layer.

iii) HMDS layer is applied using oven. This layer assists adhesion of the photoresist. Let the wafer cool for 5 minutes.

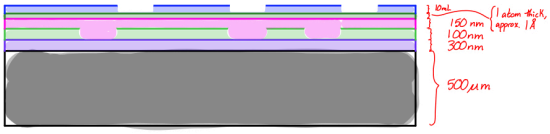
iv) Spin coat photoresist AZ 1512 onto wafer, Soft bake for 60s and let cool.



v) Expose wafer to UV light through the second mask, patterning the photoresist.

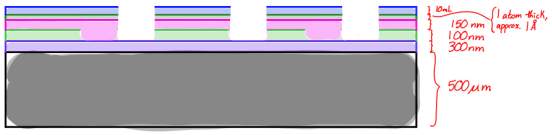


vi) Develop the wafer using AZ 400K 1:4 developer, removing exposed photoresist. The wafer must also be characterized with the microscope and alphastep.



vii) Test silicon wafer piece with nitride film and measure nitride thickness with Filmetrics F50-UV. Calculate etch time.

viii) Etch the Silicon Nitride using the Trion RIE.



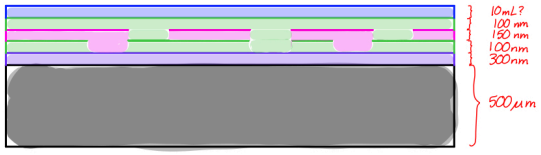
ix) Remove excess photoresist and characterize and inspect using microscope and Alphastep.

Lab 3: Process Flow Cross-Section

i) Wafer from previous lab with Silicon oxide, Aluminum and Silicon Nitride layers.

ii) Aluminum layer is sputtered onto the wafer. This is done using the magnetron sputtering system. The pattern is 'baked in' for 5min to clean the surface and then the aluminum is deposited.

iii) Photoresist (AZ1512) is spun onto the wafer and baked on. Then it is left to rehydrate for 30-60s



iv) Photoresist is patterned with the final mask. The photoresist that is exposed is softened so that it can be removed

v) The photoresist (AZ 1512) is then developed in the AZ400 1:4 developer, removing the previously exposed photoresist. The pattern must then be characterized using the microscope and AlphaStep.

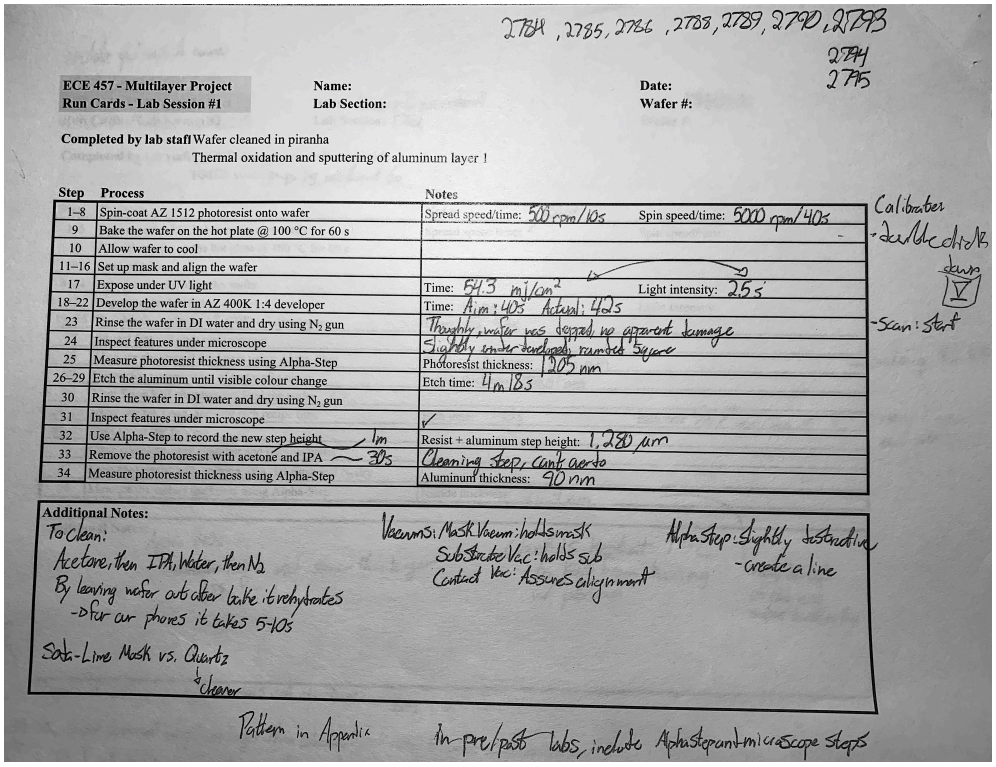
vi) Aluminum is now etched using the aluminum etchant (phosphoric acid: nitric acid: acetic acid: water). This should take 5-10 minutes. The etch is then inspected using the microscope to ensure all aluminum is removed.

vii) Photoresist is removed using acetone and IPA. The wafer should then be inspected to ensure all photoresist is removed and then measure the aluminum thickness using the Alphastep.

Appendix E: Error Analysis

Throughout the course of the lab a few instruments were used to characterize the wafer and its features. Unfortunately for the purposes of writing this report, the metrological specifications and data of these instruments are not available. Due to the rarity of these instruments and their documentation it is also difficult to just assume that they are operating within manufacturer's specifications. To compound on the lack of information about the uncertainty of these instruments, they were occasionally found to give completely incorrect or inconsistent results, either supported by the impossibility of the results or by advice of the lab instructor. This could be due to operator error on my part but has the same effect on the uncertainty. Due to these factors, error calculations have been neglected for the entirety of the report as they themselves would have uncertainty eclipsing the actual value of the measurand. The numerical values in this report still hold value relative to each other and can be used to show correlation and relationships between factors but cannot be relied on out of this context.

Appendix F: Run Cards



2784, 2785, 2786, 2788, 2789, 2790, 2793
2784
2795

ECE 457 - Multilayer Project **Name:** **Date:**
Run Cards - Lab Session #1 **Lab Section:** **Wafer #:**

Completed by lab staff Wafer cleaned in piranha
Thermal oxidation and sputtering of aluminum layer !

Step	Process	Notes
1–8	Spin-coat AZ 1512 photoresist onto wafer	Spread speed/time: 500 rpm/10s Spin speed/time: 5000 rpm/40s
9	Bake the wafer on the hot plate @ 100 °C for 60 s	
10	Allow wafer to cool	
11–16	Set up mask and align the wafer	
17	Expose under UV light	Time: 54.3 mj/cm² Light intensity: 2.5 s
18–22	Develop the wafer in AZ 400K 1:4 developer	Time: Aim: 40s Actual: 42s
23	Rinse the wafer in DI water and dry using N_2 gun	Thoughly, wafer was stepped, no apparent damage
24	Inspect features under microscope	Slightly under developed, rounded Square
25	Measure photoresist thickness using Alpha-Step	Photoresist thickness: 1205 nm
26–29	Etch the aluminum until visible colour change	Etch time: 4m 18s
30	Rinse the wafer in DI water and dry using N_2 gun	
31	Inspect features under microscope	✓
32	Use Alpha-Step to record the new step height ~1m	Resist + aluminum step height: 1,280 μm
33	Remove the photoresist with acetone and IPA ~30s	Cleaning step, can't use to
34	Measure photoresist thickness using Alpha-Step	Aluminum thickness: 90 nm

Calibrate
- double check levels
- Scan: start

Additional Notes:
To clean:
Acetone, then IPA, Water, then N_2
By leaving wafer out after bake it rehydrates
-> for our phones it takes 5-10s

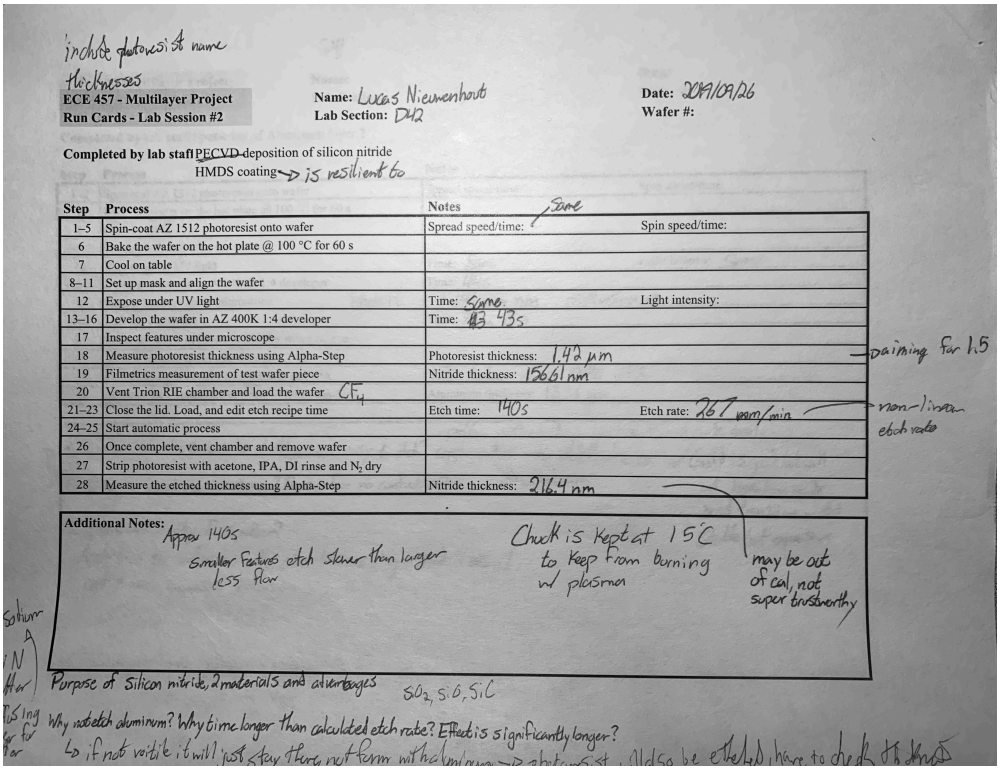
Soda-Lime Mask vs. Quartz
↓
cheaper

Vacuums: Mask Vacuum: holds mask
Substrate Vac: holds sub
Contact Vac: Assures alignment

Alpha Step: Slightly destructive
- create a line

Pattern in Appendix

In pre/post labs, include Alphastep and microscope steps



include photoresist name
thicknesses

ECE 457 - Multilayer Project **Name:** Lucas Nieuwenhout **Date:** 2019/09/26
Run Cards - Lab Session #2 **Lab Section:** D42 **Wafer #:**

Completed by lab staff ~~PECVD~~ deposition of silicon nitride
HMDS coating -> is resilient to

Step	Process	Notes
1–5	Spin-coat AZ 1512 photoresist onto wafer	Spread speed/time: Same Spin speed/time:
6	Bake the wafer on the hot plate @ 100 °C for 60 s	
7	Cool on table	
8–11	Set up mask and align the wafer	
12	Expose under UV light	Time: Same Light intensity:
13–16	Develop the wafer in AZ 400K 1:4 developer	Time: ~~43~~ 43s
17	Inspect features under microscope	
18	Measure photoresist thickness using Alpha-Step	Photoresist thickness: 1.42 μm
19	Filmetrics measurement of test wafer piece	Nitride thickness: 1566 nm
20	Vent Trion RIE chamber and load the wafer CF_4	
21–23	Close the lid. Load, and edit etch recipe time	Etch time: 140s Etch rate: 267 nm/min
24–25	Start automatic process	
26	Once complete, vent chamber and remove wafer	
27	Strip photoresist with acetone, IPA, DI rinse and N_2 dry	
28	Measure the etched thickness using Alpha-Step	Nitride thickness: 216.4 nm

- paining for 1.5
- non-linear etch rate

Additional Notes:
Appox 140s
Smaller features etch slower than larger
less flow

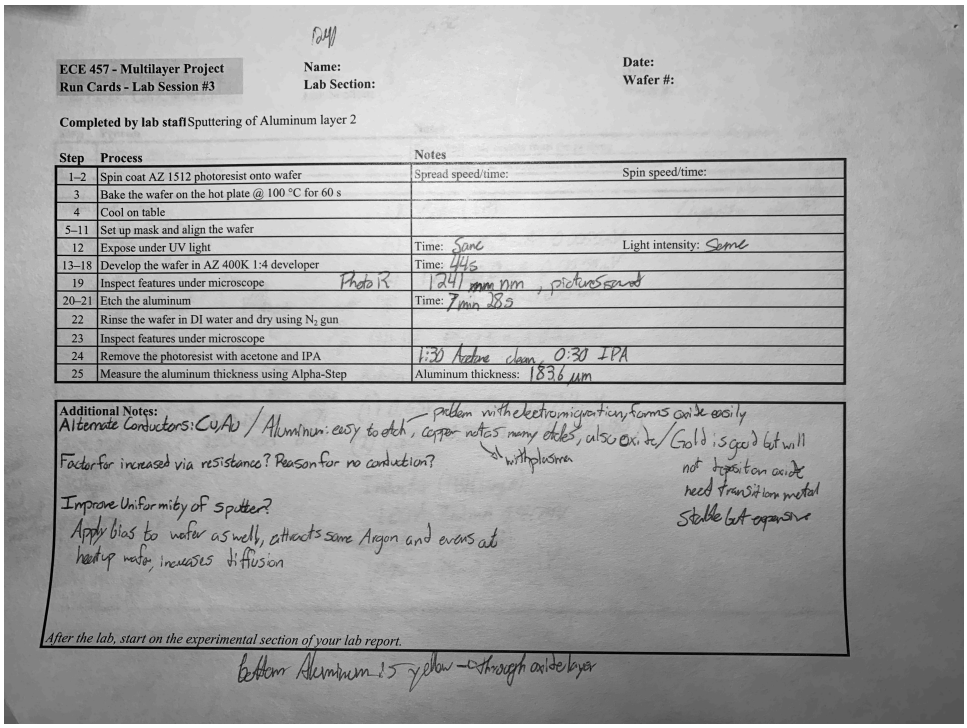
Chuck is kept at 15C to keep from burning w/ plasma

may be out of cal, not super trustworthy

Solution
N
After
ing for for

Purpose of Silicon nitride, 2 materials and advantages SO_2, SiO, SiC

Why not etch aluminum? Why time longer than calculated etch rate? Effect is significantly longer?
↳ if not visible it will just stay there, not form with the [illegible]



Lab

ECE 457 - Multilayer Project
Run Cards - Lab Session #3

Name:
Lab Section:

Date:
Wafer #:

Completed by lab staff Sputtering of Aluminum layer 2

Step	Process	Notes
1–2	Spin coat AZ 1512 photoresist onto wafer	Spread speed/time: Spin speed/time:
3	Bake the wafer on the hot plate @ 100 °C for 60 s	
4	Cool on table	
5–11	Set up mask and align the wafer	
12	Expose under UV light	Time: 5sec Light intensity: Some
13–18	Develop the wafer in AZ 400K 1:4 developer	Time: 44s
19	Inspect features under microscope Photo R	1241 mm nm, pictures saved
20–21	Etch the aluminum	Time: 7min 28s
22	Rinse the wafer in DI water and dry using N_2 gun	
23	Inspect features under microscope	
24	Remove the photoresist with acetone and IPA	1:30 Acetone clean, 0:30 IPA
25	Measure the aluminum thickness using Alpha-Step	Aluminum thickness: 1836 nm

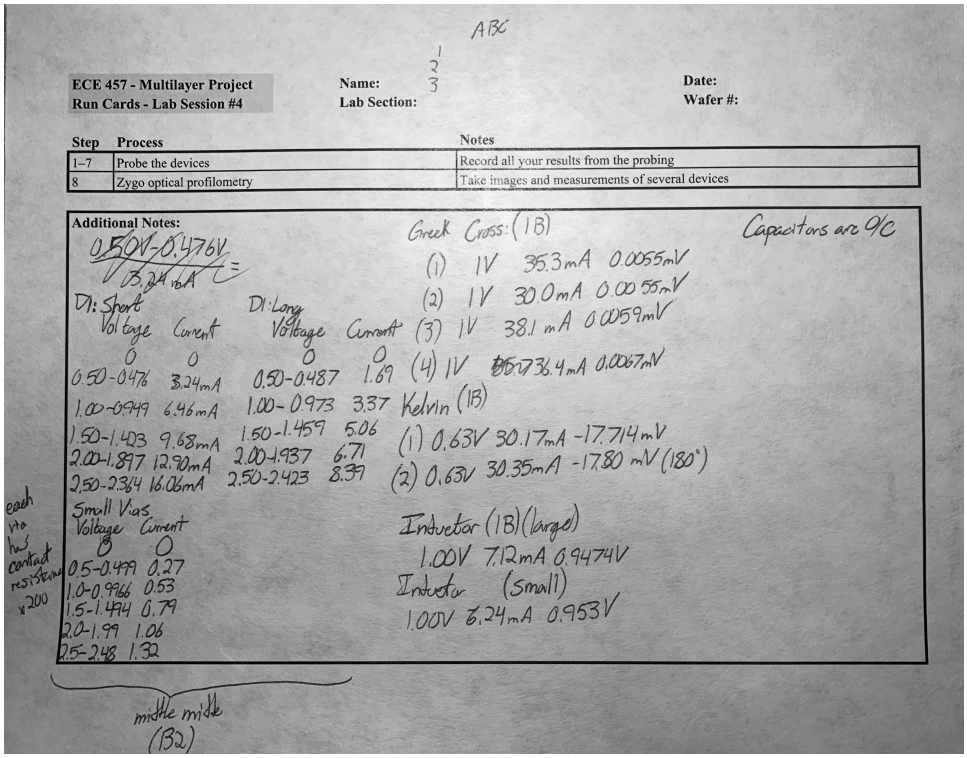
Additional Notes:
Alternate Conductors: Cu, Au / Aluminum: easy to etch, copper notes many etches, also oxide / Gold is good but will not transition oxide need transition metal Stable but expensive
problem with electromigration, forms oxide easily
with plasma

Factor for increased via resistance? Reason for no conduction?

Improve Uniformity of sputter?
Apply bias to wafer as well, attracts some Argon and evens out heating wafer, increases diffusion

After the lab, start on the experimental section of your lab report.

Bottom Aluminum is yellow — through oxide layer



ABC
1
2
3

ECE 457 - Multilayer Project
Run Cards - Lab Session #4

Name:
Lab Section:

Date:
Wafer #:

Step	Process	Notes
1–7	Probe the devices	Record all your results from the probing
8	Zygo optical profilometry	Take images and measurements of several devices

Additional Notes:

0.50V-0.476V
13.24 mA =

DI: Short

Voltage	Current
0	0
0.50-0.478	3.24mA
1.00-0.949	6.46mA
1.50-1.403	9.68mA
2.00-1.897	12.90mA
2.50-2.364	16.06mA

DI: Long

Voltage	Current
0	0
0.50-0.487	1.69
1.00-0.973	3.37
1.50-1.459	5.06
2.00-1.937	6.71
2.50-2.423	8.39

Small Vias

Voltage	Current
0	0
0.5-0.499	0.27
1.0-0.966	0.53
1.5-1.494	0.79
2.0-1.99	1.06
2.5-2.48	1.32

each via has contact resistance ~200

middle middle (132)

Greek Cross: (1B)
(1) 1V 35.3mA 0.0055mV
(2) 1V 30.0mA 0.0055mV
(3) 1V 38.1 mA 0.0059mV
(4) 1V ~~86.736.4~~mA 0.0067mV

Kelvin (1B)
(1) 0.63V 30.17mA -17.714mV
(2) 0.63V 30.35mA -17.80 mV (180°)

Inductor (1B) (large)
1.00V 7.12mA 0.9474V

Inductor (small)
1.00V 6.24mA 0.953V

Capacitors are 9C