ECE 457 - MEMS Project

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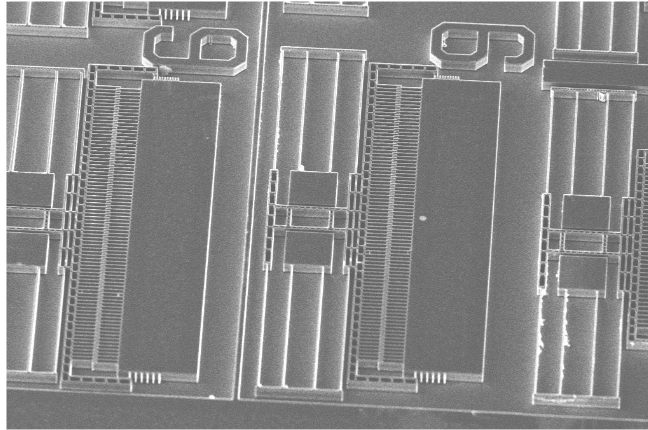


Abstract

The objective of this lab is to learn about the methods and techniques used in the fabrication of MEMS devices and use characterization equipment to test their functionality. This lab was completed using the resources of the NanoFAB at the University of Alberta with assistance from the lab staff. During our lab sessions we used typical MEMS fabrication processes on test-SOI wafers(simple Si wafers) to gain experience with the manufacturing of MEMS and then characterized a previously fabricated SOI wafer with a probe station and a scanning electron microscope. The devices on the SOI wafer included small and large comb drives, Archimedean spirals, tweezers, resistance gauges, and other various MEMS devices. We characterized a majority of the devices but focused on the comb drives because of our ability to model them. The correlation between the measured and theoretical displacement of the large and small comb drives was inconsistent. For device B4, the displacement as well as spring constant correlated closely in relationship as well as magnitude. While for device B6 and D8 the measured and theoretical values varied far more. For device B6 the theoretical spring constant was only 31% of the measured spring constant. The overall yield of our wafer was 85.71% but this is likely artificially high due to our tendency to test devices that were more likely to work. A more reasonable yield approximation might be 60-75%. The yield and correlation could be increased by developing the photoresist for a shorter time(as it appeared to have been slightly overdeveloped) or testing a higher number of devices to obtain a more representative approximation.

Introduction

Fabrication of micro- and nano-scale devices is an industry that is growing as the need for smaller, quicker, and more power efficient devices increases. These devices are needed in the market and for research purposes. The technologies and processes involved in this micro fabrication allow for granular control of many important properties of the resultant wafers. The goal of this lab is to learn the processes and techniques used in the micro fabrication of micro electro-mechanical systems(MEMS) and how they impact the final device that is created. We also learned about the characterization techniques used to inspect the devices and verify their functionality. This lab was conducted using the resources and expertise of the University of Alberta NanoFAB and its staff.

There is a wide variety of devices designed on the wafer for this lab, ranging from simple springs and comb drives to more complex inchworm gears and Archimedean spirals. All of these devices are able to be designed and manipulated because of the relatively unique structure of the Silicon-on-Insulator(SOI) wafer. This wafer structure has a silicon handle and top layer with an intermediate sacrificial insulator layer made of SiO_2. There are a few methods that can be used to construct these wafers but we believe that the method used to construct the wafer used in our lab was oxygen ion implantation followed by annealing of the wafer to create the silicon dioxide. The SOI wafer structure allows us to pattern the top silicon layer of the wafer to create our devices and then etch away a majority of the SiO_2 layer, allowing the devices to move freely except where they remain anchored by the SiO_2. Using this method we can couple the devices' electrical and mechanical properties. This means that by applying a voltage potential across a set of interdigitated capacitors we can actuate the device. The reverse is also useful as we can measure the mechanical movement of the device by measuring the change in capacitance as the interdigitated capacitors separate or come closer together.

The wafer was patterned using AZ 1529 photoresist before the top silicon layer was anisotropically etched using the Bosch process and the wafer was cleaned of any residual photoresist or C_4H_8 polymer. The sacrificial silicon dioxide layer was then isotropically etched using Vapour Phase Hydrofluoric etching to release the MEMS devices. Since our group did not actually have an SOI wafer to conduct these processes on, we used test silicon wafers for these processes. Then for the characterization portion of the lab we used a completed SOI wafer from a previous group. This was used for testing of the devices with a probe system and inspecting the features under the scanning electron microscope(SEM).

Experimental

The entirety of this lab was conducted within the University of Alberta NanoFAB located in the Electrical and Computer Engineering Research Facility. All equipment and materials used in this lab were provided by the NanoFAB and its staff. While a certain portion of the work was done by us during the laboratory section, a large amount of work was done by the lab staff between sections to allow us to continue. The steps completed by the lab staff will be indicated and described in the experimental section as relevant. References will be made to Appendix D showing the cross-section of the wafer at that point in the lab with format (L1,i) representing step i) from Lab 1. Supplemental images can be seen in Appendix B. The structure of this lab is such that we practice the manufacturing processes on four test wafers before repeating the step on the SOI wafer. Due to a shortage of SOI wafers in the lab we were not able to repeat the processes on the actual SOI wafer but the characterization was done with an SOI wafer from a previous lab section.

The manufacturing process begins with the construction of the actual SOI wafer along with the manufacturing of our test wafers. The SOI wafers are constructed using oxygen ion implantation into the wafer and then annealing to create the SiO_2 layer. This results in a wafer that has a thick 500μm silicon base, a 300nm sacrificial silicon dioxide layer, and then another thinner 100nm silicon layer on top. Due to the expensive nature of the SOI wafers, we also use simple test wafers to practice our procedures before conducting them on the SOI wafer. These test wafers are simply silicon wafers that were left from previous lab tests as their performance is not critical.(L1,i)

The SOI wafers arrive mostly clean from contaminants but there is still a possibility that other materials have adhered to the wafer or that oxides have formed on the top silicon layer. The wafer is prepared in a two step process: the wafer is cleaned for 15 minutes in a piranha solution(3:1 mixture of sulphuric acid:hydrogen peroxide), then cleaned for 2 minutes in a buffered oxide etch(BOE)(10:1 mixture of ammonium fluoride:hydrofluoric acid). The piranha solution will remove any organic materials present on the surface of the wafer and the BOE will remove any unintended oxide build up on the surface.(L1,ii) Finally a hexamethyldisilazane(HMDS) monolayer is deposited on the wafer to promote adhesion between the top silicon layer and the photoresist that is to be applied.(L1,iii) These steps were all completed by the NanoFAB lab staff prior to the lab sessions.

To pattern the wafers we used a temporary photoresist layer that was removed after the wafer was etched. A positive photoresist AZ1529 as manufactured by MicroChemicals was applied to the wafers using the Cee 200CB Coat-Bake system. The wafer was centred on the pedestal of the Cee 200CB before approximately 10-15ml of AZ1529 was poured into the centre of the wafer and the spread and spin cycle was started. This consisted of a spread recipe of 500rpm for 10s followed by 3000rpm for 60 seconds. This process increases the chance of covering the entire wafer in photoresist and then spinning at a high speed to level out the applied photoresist. After the photoresist is spin-coated onto the wafer, the wafer is baked on a hot plate at 100°C for 60s to remove excess water from he photoresist solution. The wafer is

then left to rehydrate for 10-60s, reintroducing a small amount of water to the photoresist that is required for proper exposure.(L1,iv)[1]

As we are using a positive photoresist, the regions of the photoresist that we expose to light will become more susceptible to the AZ 400K 4:1 developer and be etched to the pattern of the mask. The exposure of the photoresist was completed using the ABM Contact Mask Aligner. This allows you to align the wafers to the mask and then expose them to a precise intensity and duration of UV light. As we are only applying a single pattern to the wafer the alignment of the mask to the wafer is not critical except that we roughly centre the pattern on the wafer. The light that the photoresist is exposed to consists of UV light in the wavelengths of 365nm and 405nm. This is the range of light that will 'expose' the photoresist and the rest of the photolithography area is lit with longer wavelength light to avoid accidental exposure. The photoresist layer was exposed with an intensity of 53.5mW/cm^2 for 4.8s.(L1,v)

The wafer was then developed in the AZ 400K 1:4 developer by submerging the wafer in a glass dish containing the developer, and agitating the solution to promote development and diffusion of reactants. The UV exposed photoresist will etch at a much faster rate than the other photoresist but it is important not to over or underdeveloped the pattern. Since we had multiple test wafers that we had patterned and could develop, we decided to purposefully over- and under-develop two of the wafers so that we could examine the effect this had on the photoresist layer. Then, by examining the times that led to over- and under-development we attempted to develop two of the wafers optimally. To under and over develop the wafers we developed one wafer for 39s and the other for over 176s respectively. Using these times we then developed two wafers to find the optimal developing time that we would have used on our actual SOI wafer. By alternating developing and then inspecting the wafer with the microscope we settled on a development time of 129s for the optimal developing time where the wafer was completely cleaned of excess photoresist but was also not over-developed. Images showing the development stages can be seen in Figures 1, 2 and 3. We then measured the photoresist thickness on our pseudo-SOI wafer to be 4181nm using the AlphaStep profilometer.(L1,vi)

The second lab session is focused on the Bosch etch process and preparing the wafer for the removal of the sacrificial layer. These two steps are critical to the manufacturing of MEMS as they allow for anisotropic etching of the silicon and the releasing of the MEMS devices. Many of the processes in this lab session are predominantly done by machines without much user input but the internal processes of the systems will be explained. There are no steps taken between lab session 1 and lab session 2.

This lab session begins with the anisotropic etch of the top silicon layer of the wafer, this is meant to be the SOI wafer but since we did not have our own we carried this our on our best developed test wafer. The Bosch etch is used to etch the wafer. This process uses alternating polymer application and isotropic etching cycles to generate a virtually anisotropic etch through silicon. The process begins with a short isotropic etch using SF6, followed by application of a polymer C4F8 to cover the wafer and its features. With the next etch cycle the bottom of the features is etched much more quickly because the

sidewalls are protected by the polymer layer whereas the polymer on the bottom of the feature is removed/weakened by ion bombardment. The polymer application and isotropic etch steps are repeated until the desired depth is reached. The Bosch etching system is also load-locked. This means that there is a separate vacuum chamber specifically for loading the wafer which will then be moved over to the main etching chamber when vacuum has been reached. This reduces the contamination in the main chamber and reduces the total time as we do not have to wait for the entire chamber to be pumped down, just the load-locking chamber.

Before we etch our pseudo-SOI wafer, we condition the Bosch etch system(Oxford Estrelas ICPRIE) to ensure that we have flushed out any contaminants form previous Bosch etch cycles and that we can ensure that our process is repeatable. This is done by running 20 cycles of our process on a conditioning wafer. We then loaded the pseudo-SOI wafer into the system and ran 50 cycles of the ECE 457 Bosch Etch Process, this took approximately 140s.(L2,ii) We then measured the height that had been etched using the AlphaStep profilometer. We measured the new depth from the top of the photoresist to the bottom of the etch pattern to be 9400nm.(L2,iii) For our calculations during the lab we assumed that none of the photoresist had been etched by the process. This led to a calculated etch rate of approximately 0.104 µm/cycle as calculated in Equation 1. To etch the remaining silicon we would need 141.6 more cycles as calculated in Equation 2. This is rounded up to 145 as partial cycles are not possible and to ensure that the silicon layer is completely etched.(L2,iv) It does not matter if we etch slightly into the SiO2 layer as all of the exposed regions are to be removed by a future process.

$$EtchRate = \frac{9400nm - 4181nm}{50\ cycles} = 104.38\frac{nm}{cycle} \qquad (1)$$

$$AdditionalCyclesRequired = \frac{(20000nm - (9400nm - 4191nm))}{104.38\frac{nm}{cycle}} = 141.6\ cycles \qquad (2)$$

The additional 145 cycles of the Bosch process were conducted, taking a time of 315s. The total step height from the top of the remaining photoresist to the bottom of the etch pattern was measured using the AlphaStep to be 27569nm. The photoresist was then removed from the wafer by 127s in an acetone bath followed by isopropyl alcohol and water rinsing, and finally drying. The wafer was measured again using the AlphaStep but this time to find the height of the silicon that was etched, this was found to be 23695nm. Finally, the wafer was inserted into the Oxford NGP80 RIE(after a conditioning cycle of 2m) to be oxygen plasma cleaned. The program “ECE457 Clean” was run for 300s to clean off any remaining photoresist and polymer from the Bosch process. The wafer was inspected but found to still be dirty so it was re-cleaned for another 180s of the “ECE457 Clean” process until it was finally completely clean. (L2,vi) Our pseudo-SOI wafer is now prepared for releasing of the devices by etching of the sacrificial SiO2 layer if we had an actual SOI wafer. The SiO2 is etched using Vapour Phase HF(VHF) etching. As advertised, this process uses vapour phase hydrofluoric acid to isotropically etch the sacrificial layer and release the MEMS devices. This process is preferred over wet etching as it removes the need for liquid

etchant and essentially eliminates the possibility of stiction ruining the devices even without using critical point drying.(L2,vii)

In addition to the pseudo-SOI wafer that we manufactured properly, we completed an isotropic etch of one of the other practice Si wafers using the Oxford NGP90 RIE in a SF6 etch. This was also examined in the fourth lab session.

This completes the manufacturing process of the wafers in the NanoFAB, the remaining lab sessions focused on the characterization of the wafers and their devices. The characterization done in the third lab was done using a Wentworth Probe station to apply a voltage across the devices and observe their movement while the characterization in the fourth and final lab section focused on the use of the scanning electron microscope(SEM) to capture scans of the features. Images from the SEM can be seen in Figure 7 and 8, measuring the tooth gap of the interdigitated capacitors as well as in Figures 9 and 10 displaying the results of different etch processes.

Results

In this lab there was only a single pattern etched into the wafer, so the alignment was not critical as long as we maximized the number of complete dies on the wafer. What is quite critical though is the development of the photoresist and etching of the silicon and silicon dioxide layers. In an effort to study this and find the optimal development time we purposely over and underdeveloped a couple of our wafers. The underdeveloped wafer was developed for a total time of 39s and can be seen in Figure 1, while the overdeveloped wafer was developed for a total time of 176s and can be seen in Figure 2. With our final two wafers we aimed to develop them perfectly which resulted in a development time of 129s and results that can be seen in Figure 3.We used the properly developed wafer as our pseudo-SOI wafer and the thickness of the photoresist after development was measured with the AlphaStep to be 4181nm.

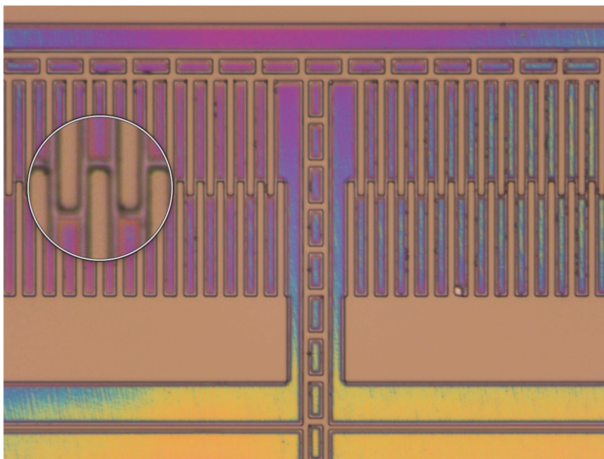


Figure 1: Underdeveloped Photoresist

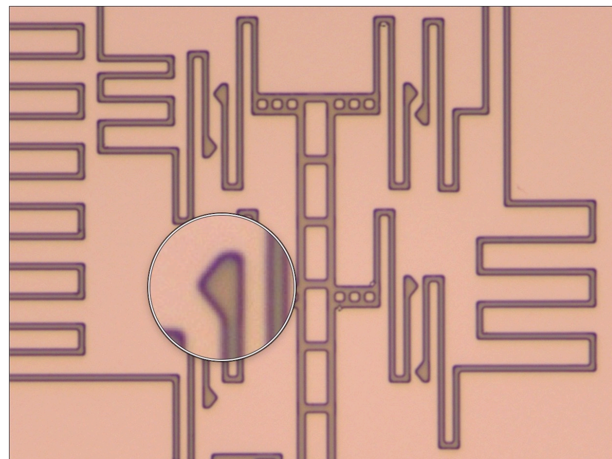


Figure 2: Overdeveloped Photoresist

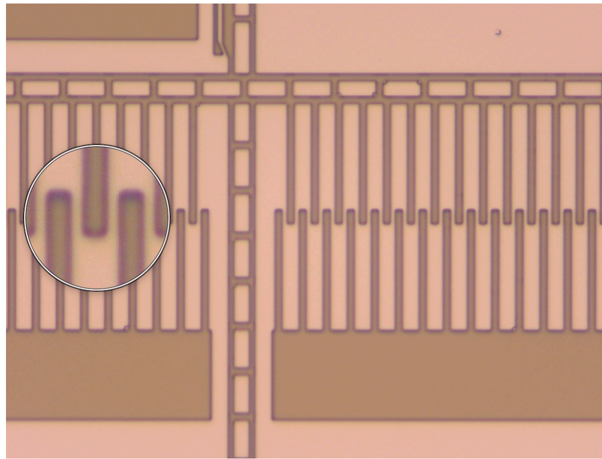


Figure 3: Properly Developed Photoresist

In the second lab the etching of the top silicon layer was completed. During and after this process we measured the thickness of the wafer to determine the etch rates of the Bosch process and the original thickness of our silicon. The calculations of etch rate can be seen below and the full derivation can be seen in Appendix C. The etch rates are calculated using the thicknesses from the first 50 cycles of the etch process as these will not be affected by a potentially different etch rate when the silicon is completely etched through.

$$Etch\ Rate(s) = \frac{5.3\mu m}{140s} = 0.038\frac{\mu m}{s} \qquad (3)$$

$$Etch\ Rate(cycles) = \frac{5.3\mu m}{50\ cycles} = 0.11\frac{\mu m}{cycle} \qquad (4)$$

The devices were then tested after the silicon dioxide layer was isotropically etched away. The total yield of the devices can be seen in Table 1. The number of indeterminate results represent the devices that we accidentally damaged during testing and it is unknown whether or not they were functional before the damage. A device was deemed functional if the appropriate components moved freely and as designed, and non-functional if the device was already broken or if it was stuck and would not move after applying a voltage.

Yield Calculations					
Device	Tested	Indeterminate	Functional	Not Functional	Yield
A	3	0	3	0	100%
B	4	1	3	0	100%
C	2	1	1	0	100%
D	1	0	1	1	50%
E	1	0	1	0	100%
F	1	0	1	0	100%
G	2	0	2	1	67%
Total	14	2	12	2	85.71%

Table 1: Summary of Device Yield

During the testing we applied a voltage potential across the devices and recorded their movement. For many of the devices we simply checked for proper movement as their properties and functions are difficult to model. For the small and large comb drives we used the displacement markers on the side of the combs to quantify the movement of the comb drive with respect to the applied voltage. This relationship can be partially described using Equation 5 for a single tooth of a comb drive with fit parameters **α** and β. By setting the fit parameters **α** = β = 1 and multiplying by the number of teeth on the comb then we can get the relationship between voltage potential and force of a comb drive.(Equation 6)

$$F_{x,single} = \frac{1}{2}\frac{\partial C}{\partial x}V^2 = \frac{1}{2}(2\alpha\epsilon_0 h g^{-\beta})V^2 \qquad (5)$$

$$F_x = \frac{1}{2}\frac{\partial C}{\partial x}V^2 = \frac{1}{2}(2\epsilon_0 h g^{-1})NV^2 \qquad (6)$$

where **α** *and β are fit parameters, ε_0 is the permittivity of free space, h is the height of the comb, g is the gap width of the comb, N is the number of teeth, and V is the voltage difference.*

Furthermore, the displacement of the comb drive can be found from the force by calculating the spring constant of the comb drive. In the axis that we are actuating the comb drive the spring coefficient can be derived and calculated as in Equation 7. Due to the configuration of the single folded-beam springs we tested in the lab(parallel and series springs) the total spring constant of our springs is equal to the spring constant of a single beam.

$$k_{device} = (\frac{1}{k_x + k_x} + \frac{1}{k_x + k_x})^{-1} = (\frac{1}{k_x})^{-1} = k_x = \frac{2Ehb^3}{l^3} \qquad (7)$$

where E is Young's Modulus, h is the height of the spring, b is the width of the spring, and l is the length of the spring.

Using the force-displacement relationship of a spring and Equations 6 and 7, we can derive the relationship between comb displacement and applied voltage potential as seen in Equation 8. We can also use this relationship to calculate the spring constant of the devices as in Equation 9.

$$x = \frac{F}{k_{device}} = \frac{\frac{1}{2}(2\epsilon_0 h g^{-1})NV^2}{\frac{2Ehb^3}{l^3}} = \frac{\epsilon_0 l^3 N}{2Egb^3}V^2 \qquad (8)$$

$$k_{device} = \frac{F}{x} = \frac{\frac{\epsilon_0 hN}{g}V^2}{x} \qquad (9)$$

where x is the displacement of the comb drive.

Using Equation 8 the theoretical displacement of the comb drive was calculated using completely theoretical values, and then with theoretical values while using the gap width as measured with the SEM. (1.581µm for B4 and B6 and 2.728µm for D8) These values were plotted against the actual displacement of the comb drives for devices B4, B6 and D8. In addition, the spring constants were calculated from the measured and theoretical data where possible. Note that for device D8 we were only able to measure a single non-zero datapoint so no trend line is shown, this figure can be seen in Appendix B. The raw measured and theoretical data can be found in Appendix A and the displacement vs. voltage graphs for devices B4, B6 and D8 can be seen in Figures 4, 5, and 6 respectively.

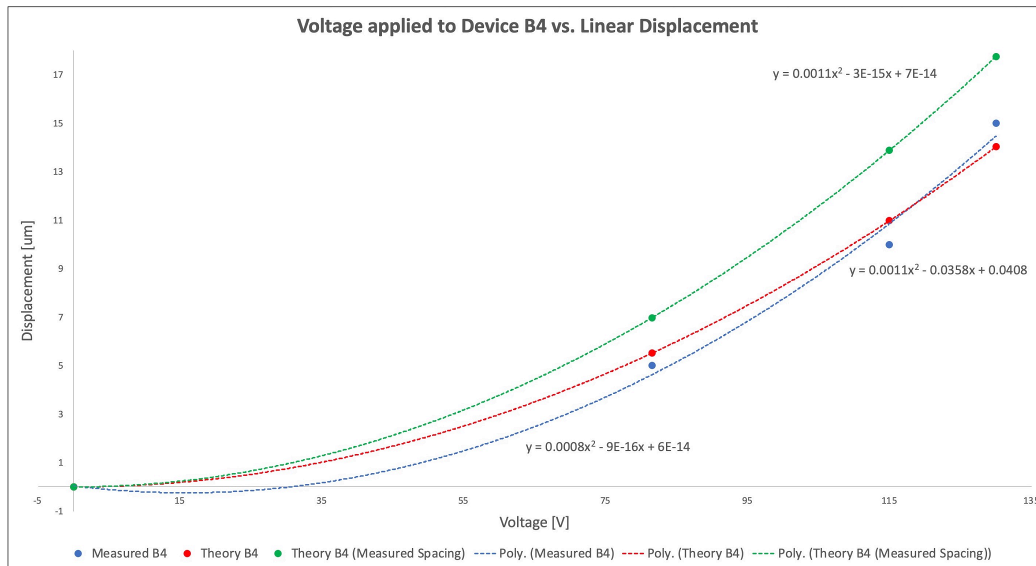


Figure 4: Voltage vs. Displacement Graph for Device B4

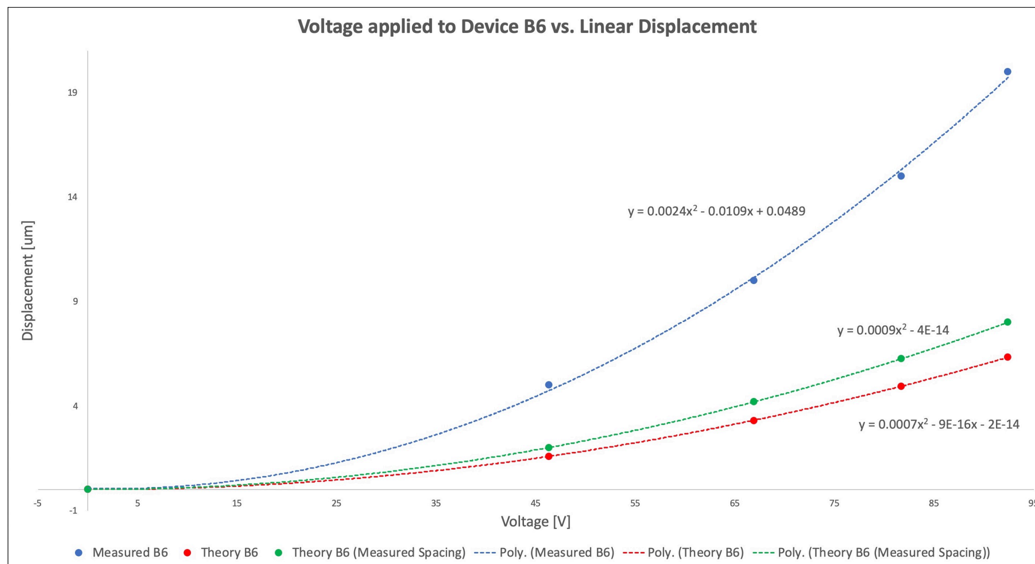


Figure 5: Voltage vs. Displacement Graph for Device B6

Discussion

The alignment of the mask on the wafer was not critical in this lab because there is only a single patterning layer, but what is critical for this lab is the development time. A proper development time ensures that the features are the correct width and length and that none of the square edges are excessively rounded. As can be seen in Figures 1, 2 and 3, we experimented with a few test wafers to find the optimal development time that should be used with our SOI wafer if one had been available. We found that a development time of approximately 129s led to the most accurate development of the photoresist and if we had an SOI wafer that is the development time that we would have used. It is also important to note that we would have the same person who developed the best test wafer also develop the SOI wafer as the agitation technique they used to develop the wafer also affects the development time. During the manufacturing of the wafers we also etched the top silicon layer in the pattern of our photoresist using the Bosch etch process. We calculated the etch rate to be 0.038µm/s or 0.11µm\cycle. These etch rates are within the expected range for the Bosch process. This is also similar but not identical to the scallop thickness measured with the SEM of 192nm as in Figure 9, a potential reason for this discrepancy is inaccurate AlphaStep measurements. In contrast to the vertical sidewalls of the Bosch etch process we also etched a silicon wafer with an isotropic SF_6 etch. It can clearly be seen in Figure 10 that this process led to significant rounding of the features and would not have been suitable for our SOI wafer as the devices deviate greatly from the design.

In the third lab section we began the characterization of the wafer using a probe setup and voltage source to actuate the MEMS devices. A majority of the devices that we tested were simply tested for functionality. This was determined by applying a voltage across the device and inspecting for resulting movement, if the device moved freely then it was considered fully functional. These devices include the

extended-needle gauges, resistance gauges, inchworm gears, springs, and tweezers. These devices serve various testing purposes from measuring the displacement of the comb drive by the resultant resistance with the resistance gauge, to allowing more precise measurement of movement using the extended needle gauge. A majority of these devices functioned as designed and could theoretically be used for their intended purpose. The yield of these devices is affected by the same factors as the comb drives.

Finally we tested small and large comb drives, which will be focused on for this discussion section as we are able to easily model the relationship between the voltage applied and distance moved. A comb drive is a simple device incorporating one or more sets of interdigitated capacitors. Applying a voltage difference across the interdigitated capacitors induces movement in the half of the interdigitated capacitors capable of movement(shuttles) and they are pulled towards the fixed half of the interdigitated capacitors(stators). The movement is measured using an indicator on the shuttle and set of markings on the side of the stator.

We tested four small comb drives and two large comb drives, one of the small comb drives was damaged during testing so its results are indeterminate and one of each of the small and large comb drives were found to not function at all. The remaining two small comb drives, B4 and B6, along with a single large comb drive, D8, were tested. Furthermore, the large comb drive we tested only resulted in a single non-zero datapoint before breaking under the applied force. The measured relationship between the voltage applied across the comb drives to the displacement of the comb drives can be seen in Figures 4, 5 and 6 for devices B4, B6 and D8 alongside the theoretical relationship as described in Equation 8. As can be seen from the plots, our measured relationship correlates quite well with the theoretical relationship for device B4 but diverges more for devices B6 and D8. There are multiple factors to explain the discrepancy which will be discussed further in this section. Ideally, the curve fitting of the data measured in the lab would result in a quadratic relationship with the quadratic term being the only non-zero term and representing the coefficient in Equation 8. This can be seen in the theoretical curve of best fit where the non-quadratic terms are practically zero.(within error of plotting program)

Using the measured data and theoretical design along with Equation 9, the theoretical and actual spring constants of the comb drives were calculated. All of the values calculated can be seen with the full measured data in Appendix A and a summary of the spring constants can be seen in Table 2. The spring constants correlate fairly well and the calculated values are in the same magnitude. The largest discrepancy between the theoretical and measured spring constants is with device B6. The measured spring constant is approximately 31% of the theoretical spring constant. There are many factors that could affect this value, a dominant factor is that device B6 was not measured starting at the zero displacement marking, but approximately a micron past this point. This would lead to overlap larger than expected in our model and the capacitive force would be higher at any point than in our theory, requiring less voltage to produce the same force.

Device	Measured Curve Fit Coefficient [µm/V]	Measured Spring Constant(Curve Fit) [N/m]	Theoretical Spring Constant [N/m]
B4	0.0011	5.721817117	7.5824
B6	0.0024	3.496666016	11.3183
D8	-	-	7.5824

Table 2: Spring Constants of Comb Drives calculated from Curve Fit and Theory

The total yield of our system was calculated to be approximately 86% as can be seen in Table 1. I believe that this is a fairly high yield for the purpose of our lab and considering that the devices were made by students. However, it should be noted that we focused on testing the devices that we knew would have a higher chance of succeeding so the true yield is likely closer to 60-75%. The devices that we predicted to have the highest yield are the small and simple ones because of their smaller surface area and less chance of a defect. Since the SOI wafer that we tested in the lab was not actually manufactured by our group in the lab it is difficult to say exactly what our largest sources of failure were but they will be discussed in general terms.

I believe that the largest cause of failure of the MEMS devices is incomplete releasing of the devices during the isotropic SiO_2 etch. This would result in the devices still being anchored to the SiO_2 in places where they should be free to move. Therefore the devices will not react to the applied voltages as expected. Failure caused by stiction is highly unlikely for our wafer as a dry HF etch was used on the sacrificial layer so no liquids were introduced onto the wafer that could potentially ruin the devices due to surface tension during drying. From inspecting the wafer during characterization it seems that all of the features were properly etched and none of the devices had features that were significantly too thin or two thick that could break under movement or impede movement entirely. During the SEM lab we measured the tooth gaps on the comb drives and found them to be slightly smaller than designed due to under-developing but the extent of the under development should only affect measured values and not cause failure. Another factor that could introduce a small discrepancy is the composition and structure of the silicon. For the calculations I assumed a Young's modulus of 160 GPa but the Young's Modulus of the actual wafer was likely different. We are unable to find out if it is higher or lower than the theoretical value but since the measured displacements tend to be higher than the theoretical displacements it is possible that the Young's modulus of our wafer is less than 160 GPa.

More specifically, with the small and large comb devices we observed acceptable yield but there were some discrepancies between the theoretical and measured values obtained in the lab. The results for device B4 correlated very well and had very similar voltage-displacement curves along with spring constants. However, for device B6 the measured displacement was much higher than the theoretical values calculated from the design dimensions. This results in the measured spring constant being much lower than the theoretical spring constants as seen in Table 2. It is strange that one device matches with theoretical very well while the other similar device has significant error. One factor of this difference could be that the devices are on different sections of the wafer and the thin film properties differ along the

wafer. Another large factor to this error is the calculation of the force applied to the comb drive. This force calculation uses the designed thicknesses, widths and overlaps of the wafer but our wafer will have different dimensions(due to over or under development and differing layer thicknesses) and thus the actual force will be different from the theoretical. As we measured the comb drive tooth gaps with the SEM to be 1.581µm and 2.782µm instead of the designed 2µm and 3µm this affects the accuracy of the calculations. Using these values for the gap widths of the comb drives we get theoretical values(Appendix A Table 3, 4, 5) that match slightly better with the measured displacements that we gathered in the lab while the theoretical spring constants remain the same as they are independent of gap width. If we had measured the thickness and length of the springs we could have calculated the theoretical spring constants considering the actual dimensions. Despite the improvement in correlation there is still significant error so clearly the other sources contribute significantly as well.

Conclusion

The main goal of this lab to learn the effect of MEMS fabrication processes and techniques was achieved through implementing the fabrication processes and then using various characterization techniques to examine the resultant wafer and devices. Multiple test SI wafers were prepared to find the best parameters for patterning of the wafer. Then the device layer of silicon was etched using the Bosch process followed by an oxygen plasma clean of the wafer and dry HF etching of the SiO_2. The wafers were then characterized in the following labs, producing a yield of 85.71% which is realistically closer to 60-75%. The theoretical and measured spring constants and displacements correlated well for device B4 but deviated quite a bit more for devices B6 and D8. The yield discrepancy, along with some of the discrepancy between theoretical and measured values could be due to slight under-development of the SOI wafer as measured with the SEM as well as modelling and calculation of the force used to determine the theoretical displacement. It is more difficult to theorize methods to improve the yield of the wafer as the wafer that we characterized was not fabricated by our group but further refining of the development time and testing a higher number of devices could lead to a better correlation between the measured and theoretical data.

Bibliography

[1] MicroChemicals, Photoresist Rehydration. Accessed Oct. 12, 2019.[Online]. https://www.microchemicals.com/technical_information/photoresist_rehydration.pdf

[2] L. Nieuwenhout, ECE 457 - Multilayer Project. Oct 17, 2019.

Appendices

Appendix A - Full Measured Data

Device B4						
Voltage (V)	Measured [um]	Theory (Measured Spacing) [um]	Theory [um]	Spring Constant (Measured) [N/m]	Spring Constant (Theory, Measured Spacing) [N/m]	Spring Constant (Theory) [N/m]
0	0	0	0	-	-	-
81.5	5	6.9748	5.5136	8.3613	7.5824	7.5824
115	10	13.8872	10.9778	8.3238	7.5824	7.5824
130	15	17.7462	14.0284	7.0912	7.5824	7.5824

Table 3: Device B4 Displacements and Spring Constants

Device B6						
Voltage (V)	Measured [um]	Theory (Measured Spacing) [um]	Theory [um]	Spring Constant (Measured) [N/m]	Spring Constant (Theory, Measured Spacing) [N/m]	Spring Constant (Theory) [N/m]
0	0	0	0	-	-	-
46.3	5	2.0107	1.5894	3.5980	11.3183	11.3183
66.9	10	4.1979	3.3184	3.7559	11.3183	11.3183
81.7	15	6.2607	4.9491	3.7344	11.3183	11.3183
92.4	20	8.0080	6.3303	3.5824	11.3183	11.3183

Table 4: Device B6 Displacements and Spring Constants

Device D8						
Voltage (V)	Measured [um]	Theory (Measured Spacing) [um]	Theory [um]	Spring Constant (Measured) [N/m]	Spring Constant (Theory, Measured Spacing) [N/m]	Spring Constant (Theory) [N/m]
0	0	0	0	-	-	-
40	-	1.6228	1.4757	-	7.5824	7.5824
81.5	10	6.7370	6.1262	4.6451	7.5824	7.5824
115	-	13.4137	12.1976	-	7.5824	7.5824
130	-	17.1412	15.5871	-	7.5824	7.5824

Table 5: Device D8 Displacements and Spring Constants

Appendix B: Additional Figures

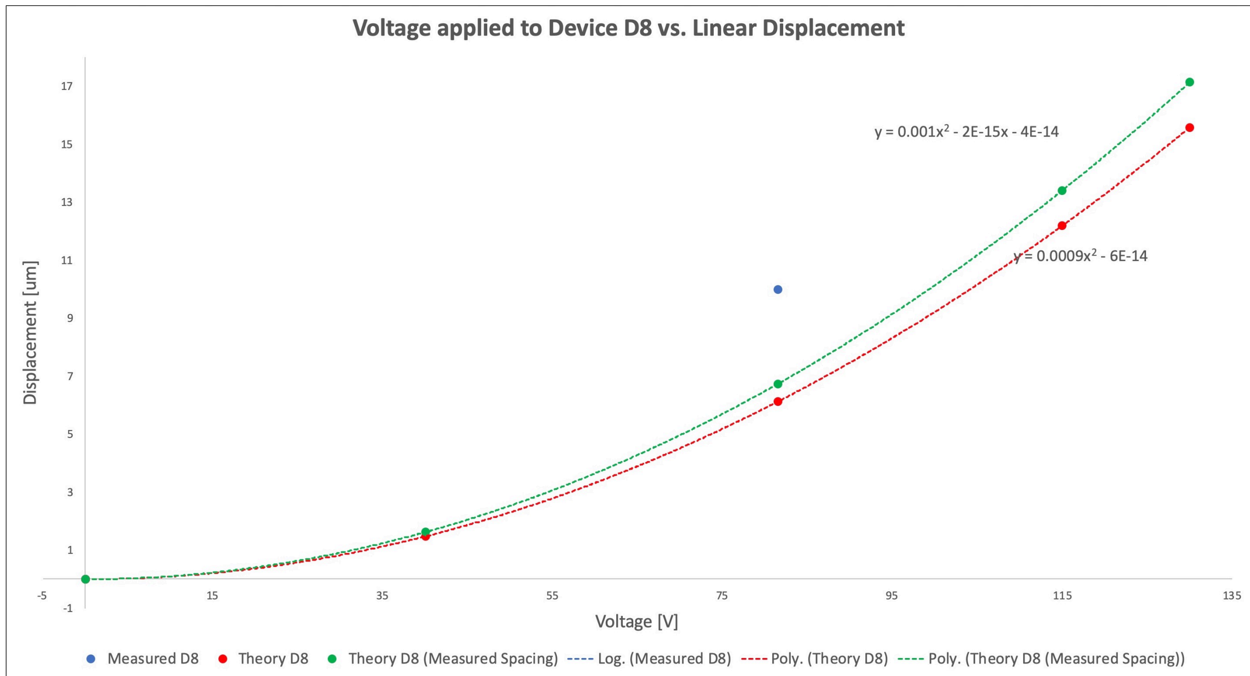


Figure 6: Voltage vs. Displacement Graph for Device B6

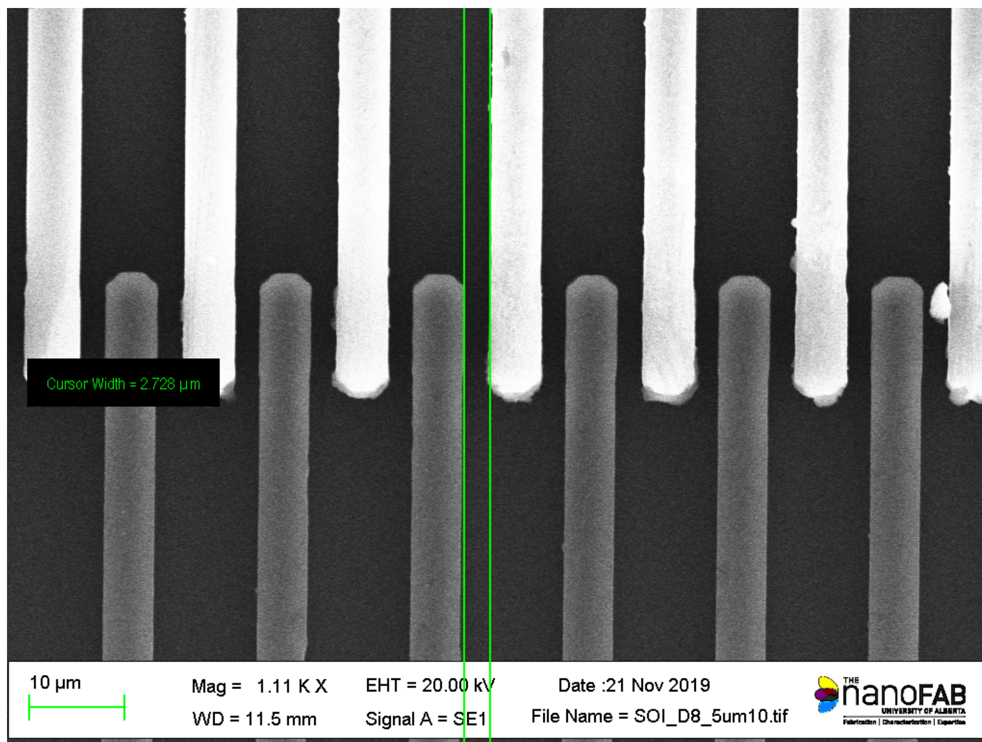


Figure 7: SEM image of tooth gap for 3µm comb drive

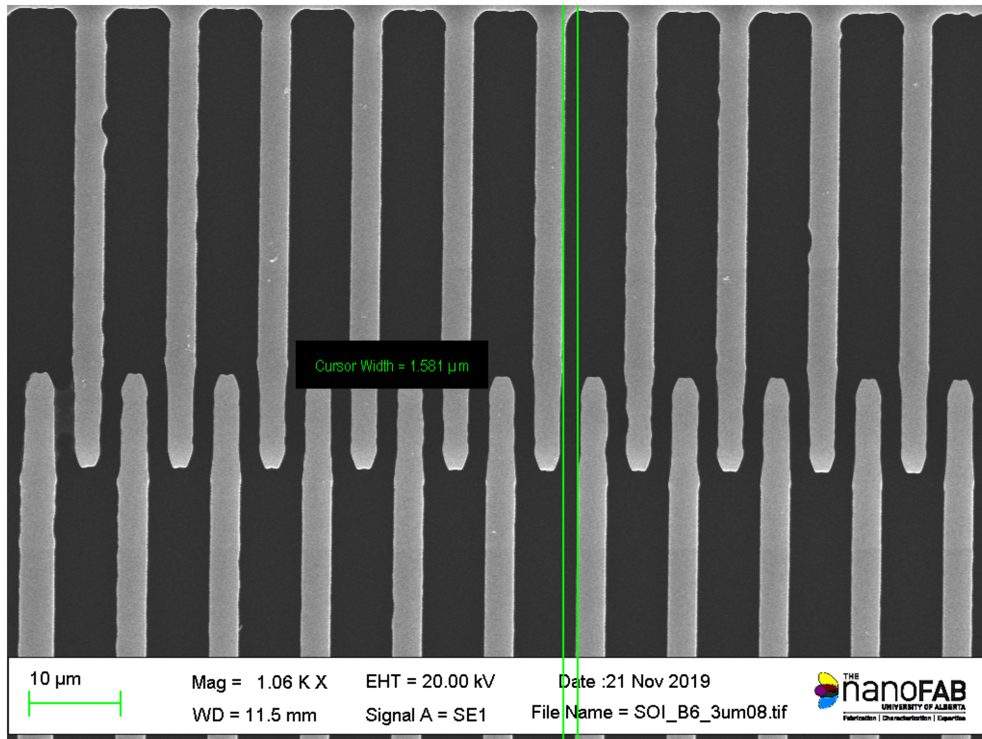


Figure 8: SEM image of tooth gap for 5µm comb drive

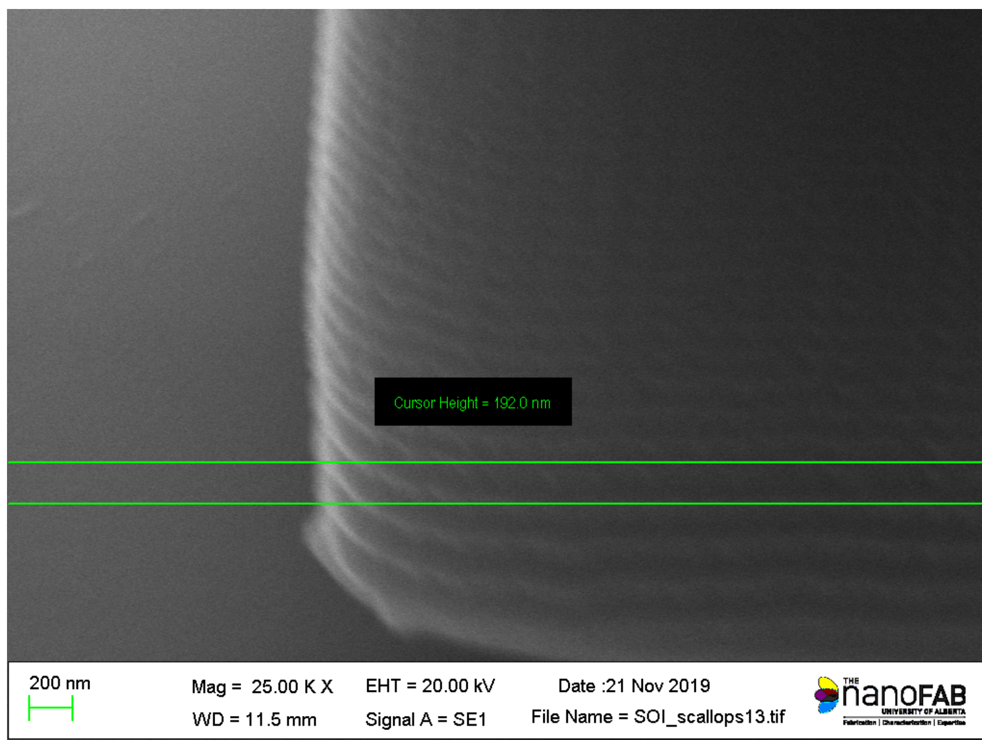


Figure 9: SEM image of etch scallops as a result of Bosch Etch Process

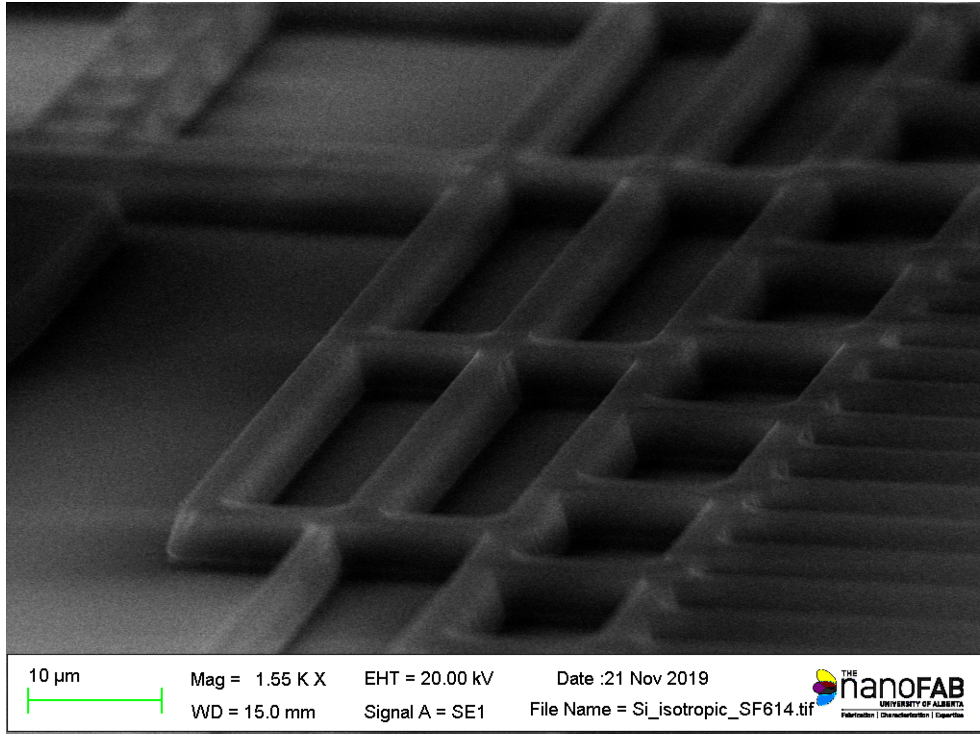


Figure 10: SEM image of isotropic SF_6 etch of silicon wafer

Appendix C: Additional Etch Rate Calculations

Measured Heights and Thicknesses:

$Initial\ Photoresist\ Height = 4.181\mu m$

$Photoresist\ and\ Silicon\ Thickness(After\ 50\ Cycles) = 9.4\mu m$

$Photoresist\ and\ Etched\ Silicon\ Thickness(After\ 195\ Cycles) = 27.569\mu m$

$Depth\ of\ Etch\ After\ Photoresist\ Removal = 23.595\mu m$

$Final\ Photoresist\ Height = 27.569\mu m - 23.695\mu m = 3.874\mu m$

Calculation of Etched Thicknesses:

$$Photoresist\ Etched\ Over\ 195\ Cycles = 4.181\mu m - 3.874\mu m = 0.307\frac{\mu m}{195\ cycles}$$

$$Photoresist\ Etched\ Over\ 50\ Cycles = 0.307\frac{\mu m}{195\ cycles} * \frac{50\ cycles}{195\ cycles} = 0.0787\mu m$$

$$Silicon\ Etched\ in\ the\ first\ 50\ Cycles = 9.4\mu m - (4.181\mu m - 0.0787\mu m) = 5.3\mu m$$

Calculations of Etch Rates:

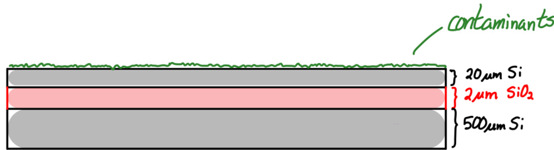
$$Etch\ Rate(s) = \frac{5.3\mu m}{140s} = 0.038\frac{\mu m}{s}$$

$$Etch\ Rate(cycles) = \frac{5.3\mu m}{50\ cycles} = 0.11\frac{\mu m}{cycle}$$

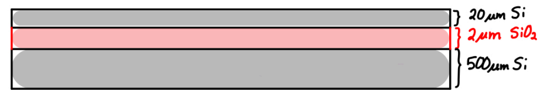
Appendix D: Full Process Steps

Lab 1: Process Flow Cross-Section

i) Start with SOI wafer, may have contaminants or other unintended materials



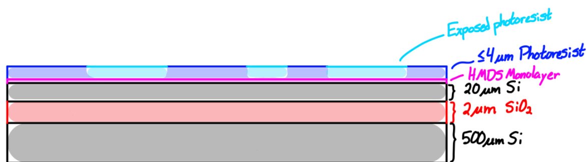
ii) Wafer is cleaned 15 minutes in Piranha Solution and 2 minutes in BOE to clean organic material and oxides off of wafer.



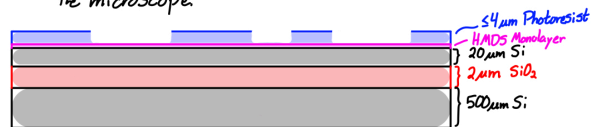
iii) HMDS layer is applied using HMDS oven. This assist adhesion between wafer and the photoresist.

iv) AZ 1529 photoresist is applied on top of HMDS layer in Spread and spin cycles, baked, and then left to rehydrate for 1 minute.

v) Photoresist is exposed to UV light on ABM mask aligner. Exposed to 250 mJ/cm^2 of light.

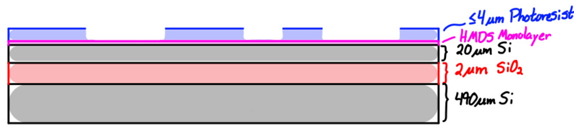


vi) Photoresist layer is developed in bath of AZ 400K 1:4 developer. Exposed regions are removed. The photoresist development is then characterized under the microscope.

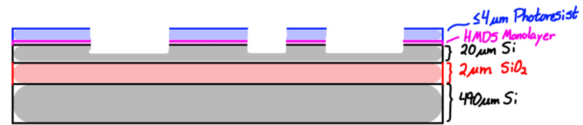


Lab 2: Process Flow Cross-Section

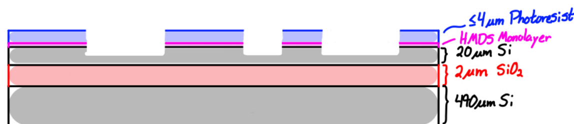
i) Begin with wafer from previous lab. This has been patterned with photoresist. This may have to be bonded to a wafer carrier for loading.



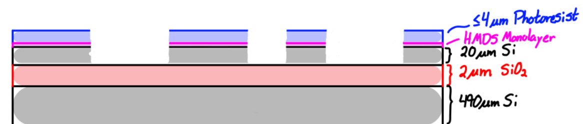
ii) Insert the wafer into the RIE system (which has been pre-conditioned). This is etched with 150-200 cycles of Bosch etching.



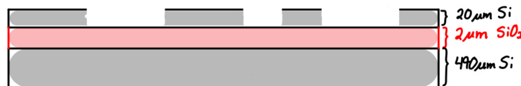
iii) The wafer is then measured using the Alphastep and the number of additional etch cycles is determined from the change in height.



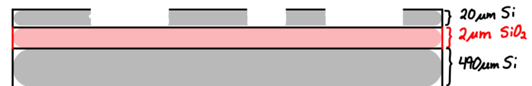
iv) Complete the Bosch etch process by etching the remainder of the top silicon layer



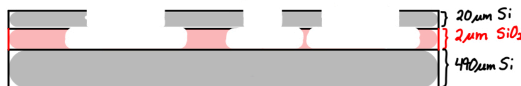
v) Remove from wafer carrier if required and remove the photo resist layer using acetone. Wafer is also cleaned with oxygen plasma clean to remove any residual polymer.



vi) Rinse and dry wafer before finally characterizing the wafer.



vii) SiO_2 is dry HF etched to release Si devices and prepare for characterization



Appendix E: Error Analysis

In this lab we used a few instruments to characterize the wafer, the devices and their features. Unfortunately the metrological specifications and data are not available to be able to calculate the proper calculation uncertainties. Furthermore, due to the rarity of these instruments their documentation is difficult to find and it is a stretch to assume that they are operating under manufacturer's specifications even if they were known. The Alphastep Profilometer was also found a couple of times to give data that completely did not agree with other more accurate instruments. This could be due to operator error or malfunction of the equipment but either way the result is that significant error is introduced into the measurement. Due to these factors error calculations are neglected for the entirety of this report as any values given would be poor guesses at best. The numerical values in this report are meaningful relative to each other and can be used for the sake of comparison and discussion but they should not be used outside of the context of this report.[2]

Appendix F: Run Cards

ECE 457 - MEMS Project
Run Cards - Lab Session #1

Name: Lucas N
Lab Section:
Date:
Wafer #:

Completed by lab staff: Wafer cleaned in piranha and BOE dip

thicker, harder etching

Step	Process	Notes	
1–7	Spin-coat AZ 1529 photoresist onto Si test wafer (3-4µm)	Spread speed/time: 10s / 500rpm	Spin speed/time: 60s / 3000 rpm
8	Bake the Si wafer on the hot plate @ 100 °C for 60 s		
9	Allow the Si wafer to cool		
10–15	Set up mask and align the Si wafer		
16	Expose under UV light	Time: 4.8s	Light intensity: 53.5 mJ/s Best
17–21	Develop the Si wafer in AZ 400K 1:4 developer	Time: 34s → underdevelop	
22	Rinse the Si wafer in DI water and dry using N_2 gun		
23	Inspect features under microscope		
24	Measure photoresist thickness using Alpha-Step	Photoresist thickness: (Jacob's Wafer): 4181 nm	
25	Spin-coat AZ 1529 photoresist onto SOI wafer	Spread speed/time: 10s/ 500 rpm	Spin speed/time: 60s/3000 rpm
25	Bake the SOI wafer on the hot plate @ 100 °C for 60 s		
25	Set up mask and align the SOI wafer		
25	Expose under UV light	Time: 4.8s	Light intensity: 53.5m /s
25	Develop the SOI wafer in AZ 400K 1:4 developer	Time: 115s + 14s	
25	Rinse the SOI wafer in DI water and dry using N_2 gun		
25	Inspect features under microscope and Alpha-Step	Photoresist thickness: 4181nm	

Additional Notes:
Jacob → "Underdeveloped" → Properly developed
Jared → Over developed →
→ 51+12+20+93

$\frac{9.4-4.2}{50} = 0.102$ µm/cycle

$\frac{(20-(9.4-4.2))}{0.102} = 145$ cycles → for SOI add 10

ECE 457 - MEMS Project
Run Cards - Lab Session #2

Name:
Lab Section:
Date:
Wafer #:

Bosch Process - Oxford Estrelas ICPRIE (27569 nm)

Step	Process	Notes	
1–2	Preform a conditioning run on blank conditioning wafer	Recipe: Bosch	Time/Cycles: ~~50~~ 20 (1-2 minutes)
3–5	Vent load-lock, remove Si, load SOI, pump down		
6–7	Run Bosch process for ~100 cycles	Cycles: 50, 2m 20s	
8	Measure etch depth using Alpha-Step	Photoresist + etched Si thickness: 9.4µm → assuming no PR etch	
9	*Calculate remaining etch cycles*	*Etch cycles remaining:* 145 cycles	
9	Repeat steps 1–4 with remaining etch cycles	Recipe: Bosch	Time/Cycles: 5m 15s/145
10–11	Strip remaining resist with acetone + IPA, rinse, dry	Time: 2m 7s	
12	Inspect features under microscope and Alpha-Step	Si thickness: 23695 nm	

Polymer Ashing and Isotropic Si Etch - Oxford NGP80

Step	Process	Notes	
13–14	Pre-clean RIE with oxygen plasma	Recipe: ECE457 Clean	Time: ~~5m~~ 2m
15	Vent the chamber and load SOI wafer		
16	Close lid and run oxygen plasma clean	Recipe: (↳ Another 3 minutes)	Time: 5m
17–20	Vent, remove SOI		
21	Load best practice Si wafer into RIE, pump down		
22	Run SF_6 isotropic etch recipe	Recipe: ECE 457 SF6	Time: 3m
24	Remove wafer and pump down NGP80		
25	Inspect features of Si and SOI under microscope	To check for cleanliness	

SF_6 for etch
C_4F_8 to polymer

Additional Notes:
For 20µm of SiO_2, 1µm of PR
Purple SF_6
Blue C_4F_8
For Actual wafer, etch longer to ensure no Si on bottom of features
Bosch only works on Si
SiO_2 where not intended might be because of contaminants or not enough Si etch
Anisotropic etches depend on crystalline structure

Now that all the fabrication steps are completed, consider starting your lab report

Calculate etch rate, selectivity of films?
Why Conditioning? → coats with polymer, covering any contaminants
Turbomolecular, why? → Cryo is low volume
Potential wet etch to use? 2 Ad and 2 dis
↳ Notes Anisotropic
One wafer is just etched with SF_6

ECE 457 - MEMS Project
Run Cards - Lab Session #3

Name: Lucas Nieuwenhout
Lab Section:
Date:
Wafer #:

Completed by lab staff: VHF release of SiO_2 sacrificial layer

Step	Process	Notes
1–3	Set up Wentworth Probe Station	
4–6	Apply a voltage to small and large comb drives	
7–9	Test inchworm gears, micro-grippers, spiral drive, etc.	

Additional Notes:

Device: D8

[μm]	[V]
0	0
5	
10	67.8 VAC D8
15	
20	

B4
5μm 81.5VDC
10μm 115 VDC
15μm 130VDC ±10V

B6
5μm 46.3VDC
10μm 66.9VDC
15μm 81.7VDC
20μm 92.4VDC

larger or more features less chance of success

C2 Extended needle shows amplified displacements

F2 worked (more than others broke)

E3

Archimedian Spiral 1
Not working

Tweezers
Two worked

D7
didn't really work

A1
Springs worked
A1, A2, A5 worked

Gate worked

A W W W
B W W
C W
D W F
E W
F W
G W W F

Calc Device yield?

Working 1 | not working

11 W 2F
12W 2F 2broken

Highly p-doped Si

ECE 457 - MEMS Project
Run Cards - Lab Session #4

Name:
Lab Section:
Date:
Wafer #:

Conductor. Can just say that actual thickness are larger, don't have to do calculations.

Step	Process	Notes
Wafer Preparation		
1	Using a diamond scribe, practice cleaving a blank Si wafer	
2	Cleave SF_6-etched Si wafer into small square/one die	
3	Attach to SEM stub with carbon tape	
4	Repeat steps 2–3 with SOI wafer	
5	Pump down SEM and load samples	
6–7	*Your Lab Instructor will take images of the devices*	

Additional Notes:

Required images for Post-Lab 4:

- Contrast too high and too low Si
- Brightness too high and too low
- 3 μm teeth and 5 μm teeth
- Sidewall
- Device disabling defect
- Archemedian spiral drive
- Tilted images
- Anything you think is neat!

Bosch
1. Si good one - aniso Si
2. Si Brightness - low brightness
3. Si Brightness - high brightness
4. Si Con low - Low
5. Si Con high - high

SOI
6. Device B6, 3μm teeth "SOI B6_3μm"
7. Device B6, gap
8. D8 "SOI_D8_5μm"
9. Scallops
10. Scallops width 192nm?

SF_6 Si
11. Si_isotropic_SF_6 → showing steps

Tungsten filament to release e^-
focused by magnetic lens'
We read backscattered and secondary e^-
→ see internal graining → can increase depth by increasing energy
→ we do this because they are only from surface, we want that

Residue on actual SOI

Dust could be device disabling

B6: 3.268μm teeth